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Présentée par :

ZOBIRI Oussama

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Contribution study of Meso-Scale Modelling and Simulation of Heat transfer phenomenon in Semiconductor Systems

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M. Boubaker Benhaoua	Professeur	Univ. El-Oued	Président
M. Kamal Mohammedi	Professeur	Univ.Boumerdes	Examinateur
M. Hocine Benmoussa	Professeur	Univ.Batna 2	Examinateur
M. Ali Boukhari	MCA	Univ .El-Oued	Examinateur
M. Redha Meneceur	MCA	Univ.El-Oued	Examinateur
M. Atia Abdelmalek	MCA	Univ.El-Oued	Dir.de Thèse

Thèse préparé au sein du **L**aboratoire d'**E**xploitation et de **V**alorisation des **R**essources **E**nergétiques **S**ahariennes

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الملخص : يعتبر الترانزستور العمود الفقري لإلكترونيات أشباه الموصلات في الوقت الحالي لتطبيقاته الواسعة في مجال تضخيم الإشارات الإلكترونية أو تبديلها. و من أشهر الترانزستورات و أكثرها إستخداما هي ذات التأثير الميداني و التي تعرف بإسم ترانزستور أكسيد السليكون ذو البوابة المعزولة (MOSFET). في السنوات الأخيرة ، اكتسب تصغير MOSFET اهتمامًا كبيرًا. و مع انخفاض حجمه (مقياس النانو) ، تؤثر الحرارة المتولدة على كفاءة الجهاز بشكل رئيسي. في هذه الأطروحة ، تم الإهتمام بنمذجة ومحاكاة نقل الحرارة في أجهزة MOSFET باستخدام طريقة شبكة بولتزمان LBM،هذه الطريقة مكنتنا من دراسة تأثير المعلمات الفيزيائية المختلفة على نقل الحرارة في أجهزة الترانزستور مثل شرط روبن الحدي وطول القناة ومعلمة الانعكاسية ونوع المادة المستخدمة دون الحاجة لإضافة حدود أخرى للنموذج الرياضي كما هو الحال بالنسبة للنمذجة الرياضية بمقياس الماكروسكوبيك. أظهرت النتائج التي تم الحصول عليها أن كل هذه المعلمات لها تأثير على شكل انتشار الحرارة وبالتالي على أداء MOSFET . أيضا أكدت النتائج على قدرة طريقة بولتزمان الشبكية LBM على المحاكات الجيدة لإنشار الحرارة داخل الأجهزة الإلكترونية المدروسة.
الكلمات المفتاحية: انتقال الحرارة ، MOSFET ، النمذجة، المحاكاة ، طريقة بولتزمان الشبكية

Abstract: The transistor is currently the backbone of semiconductor electronics for its wide applications in the field of amplification or switching of electronic signals. One of the best-known and widely used transistors is the field effect transistor, known as the insulated gate silicon oxide transistor (MOSFET). In recent years, the miniaturization of MOSFETs has attracted a lot of attention. With its reduced size (nanoscale), the heat generated mainly affects the efficiency of the device. In this thesis, the modeling and simulation of heat transfer in the MOSFET using the lattice Boltzmann method is carried out. This method allowed us to study the effect of different physical parameters on heat transfer in transistors such as Robin boundary condition, channel length, reflectivity parameter and type of material used without the need for adding extra mathematical terms. The obtained results showed that all these parameters have an effect on the diffusion of heat and therefore on the performance of the MOSFET. In addition, the results confirmed the ability of the LBM method to simulate the diffusion of heat inside the electronic devices studied.

Key words: Heat transfer; MOSFET; Modeling; Simulation; Lattice Boltzmann Method

Résumé : Le transistor est actuellement l'épine dorsale de l'électronique semi-conductrice pour ses larges applications dans le domaine de l'amplification ou de la commutation de signaux électroniques. L'un des transistors les plus connus et les plus utilisés est le transistor à effet de champ, connu sous le nom de transistor à l'oxyde de silicium à grille isolée (MOSFET). Ces dernières années, la miniaturisation des MOSFET a attiré beaucoup d'attention. Avec sa taille réduite (nanoscale), la chaleur générée affecte principalement l'efficacité de l'appareil. Dans cette thèse, la modélisation et la simulation des transferts de chaleur dans le MOSFET en utilisant la méthode Boltzmann sur réseau est effectué. Cette méthode nous a permis d'étudier l'effet de différents paramètres physiques sur le transfert de chaleur dans les transistors tels que la condition aux limites de Robin, la longueur de canal, le paramètre de réflectivité et le type de matériau utilisé sans avoir besoin d'ajouter d'autres termes au modèle comme le cas du modèle mathématique macroscopique. Les résultats obtenus ont montré que tous ces paramètres ont un effet sur la diffusion de la chaleur et donc sur les performances du MOSFET. Les résultats ont également confirmé la capacité de la méthode LBM à simuler la diffusion de la chaleur à l'intérieur des dispositifs électroniques étudiés.
Mots clés : Transfert de chaleur, MOSFET, Modélisation, Simulation, Boltzmann sur réseau.

Dedication

To my parents,

To my family,

To my friends

ACKNOWLEDGMENTS

First, we thank **ALLAH**, our creator for giving us the strength to do this work.

I want to express my sincere gratitude to my supervisor **Dr. A. ATIA (UEHL)**, for his excellent guidance, valuable advice, strong support, and continuous encouragement throughout the course of this research work at El Oued University. It has been a great pleasure and privilege to work under his supervision toward completion of this research.

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Nomenclature

c	lattice velocity, m s^{-1}
L_c	Channel length, m
C	Volumetric heat capacity, J m^{-3} K^{-1}
g	Phonon distribution function
$\hbar$	Planck constant divided by 2π, J s
k	Thermal conductivity, W m^{-1} K^{-1}
Kn	Knudsen number, Λ/L_c
k_B	Boltzmann constant, J K^{-1}
a	Adjustable coefficient
q_v	Heat generation rate per unit volume, W m^{-3}
u	Phonon energy density, J m^{-3}
v	Phonon group velocity, m s^{-1}
t	Time, s
T	Temperature, K
x, y	Directions, m

Greek Letters

θ_D	Debye temperature, K
Λ	Phonon mean free path, m
η	Number density of oscillators, m^{-3}
τ	Phonon relaxation time, s
ω	Phonon frequency, s^{-1}

Subscripts

i	Discrete direction
w	Wall

Superscripts

eq	Equilibrium
*	Dimensionless

Abbreviations

BTE	Boltzmann Transport Equation
CV	Cattaneo-Vernotte
DPL	Dual Phase Lag
LBM	Lattice Boltzmann Method
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
SPL	Single Phase Lag
SOI	Silicon-On-Insulator
TJBC	Temperature Jump Boundary Condition

General introduction

In recent years, with hundreds of millions of semiconductors assembled on a chip area no larger than a few square centimeters miniaturization of integrated circuits and the current trend toward Nano-scale electronics have led to tremendous integration levels. The most common type of insulated gate Field Effect Transistor (FET) which is used in many different types of electronic circuits is called the Metal Oxide Semiconductor Field Effect Transistor (MOSFET). This device has an important role in controlling the electrical current passing through it[1, 2].

In present integrated circuits, the feature size of electronic devices is comparable or even less than the mean free path of the phonon on which the transistors are built [1-4]. MOS transistors were influenced by this miniaturization and the MOSFET channel region has become smaller than the phonon mean free path [5]. To analyze the efficiency of integrated circuits consisting of transistors, the study of thermal transfer within the nano MOSFET is very important to demonstrate the thermal stability of the devices and its efficiency [6, 7]. In ultra-small semiconductor devices, the heat generated by the Joule effect can be very high as the operation power of the device cannot be reduced under a certain value [5]. Moreover, switching time of MOSFET devices reaches the phonon relaxation time, which is less than 100 ps in silicon[4, 8-10]. It is well-known that micro-nano scale heat transfer can be considerably different from Fourier's law because of the limited relaxation time of heat carriers [11]. The Boltzmann transport equation (BTE) and Monte Carlo (MC) solution method are applied to investigate the thermal transfer mechanism in structures from meso to macro-scale ,where the meso-scale method produces statistical information (the particle distribution function) in sub-continuum medium due to the movement of particle (vibration) and then we find macro-scale variable physic by collecting the functional distributions [12-14]. Besides the Joule effect (heat source), another heat source appears in the nano-MOSFET. This source stems from the phonon-wall collision at the MOS transistor interface and is expressed as temperature jump boundary condition (TJBC) [9, 15].

Many numerical and theoretical predictions of thermal behavior inside nano-MOSFETs have been reported whereas most of these studies are based on macroscopic models such as SPL, DPL and BDE [8, 16-18]. Apparently, these models require additional terms such as single and dual

phase-lag in order to give out reasonable results. Thus, the addressed challenge in this work is to test the presented mesoscopic thermal model based on lattice Boltzmann equation ability to predict nano-heat transfer process compared with the macroscopic models. The advantage of this model is that there is no need of any additional terms on one hand. On the other hand, Lattice Boltzmann method (LBM) is considered a highly efficient method for studying thermal transfer inside structures compared to macroscopic methods, especially in the nanostructure. This is because the media is sub-continuum (not continuous) in the presence of phonons (vibration of particles) and collisions between them [3, 10, 19-21]. The present work has the aim to perform an analysis in terms of thermal stability MOS transistors utilizing lattice Boltzmann model employed with the boundary condition of temperature jump. The considered model was compared with the simulation data retrieved from previous studies.

The organization of the work can be summarized as: A general introduction to nanotechnology MOSFETs devices is described in Chapter I . Then, Chapter II is an introduction to the chosen computational methodology, the Lattice Boltzmann Method (LBM). In this chapter, it will introduce the methodology and general concepts of LB method. In Chapter III , results and discussion are reported the effect of channel length and Robin boundary condition on the mechanism of heat transport in transistors devices. The numerical scheme employed for this study is based on Lattice Boltzmann Method (LBM) for heat transfer in MOS transistors. In Chapter IV presents a numerical simulation study of heat diffusion in transistors devices based on graphene material with effect specularity parameter coupled with temperature jump boundary condition .

Chapter I: State Of The Art :Metal Oxide Semiconductor Field Effect Transistor (MOSFET) Nanotechnology

I.1 Introduction

Although one could say that the electronics age started with Braun's cathode ray tube (1897) and Fleming's vacuum tube rectifier (1904), the real electronics era began with Lee de Forest's triode, where they transformed Fleming's rectifier as an amplifier. The use of triode (amplifier) in the field of communications led to amazing success and communication became a reality, but a problem emerged in this device is the consumption of a lot of energy. In the mid-1920s, Julius Lilienfeld began his work on finding a solid-state replacement for the triode [22].

In 1930 and 1933, Julius Lilienfeld obtained patents for devices resembling today's MESFET and MOSFET, respectively. In 1934 Oskar Heil made a theoretical work on capacitive control for field-effect transistors (FETs) [23]. When manufacturing a MOSFET, we must give importance to the effect of heat transport due to low channel region and reduction size of device especially since it has become on nano-scale [5, 18].

I.2 MOSFET

I.2.1 A conventional MOSFET

A shown in Fig I.1, a conventional MOSFET device consists of a channel connecting the source to the drain, a gate located on top of the channel, a gate oxide (insulator) between the gate and the channel, which blocks the electrical current from the gate to the channel [24].

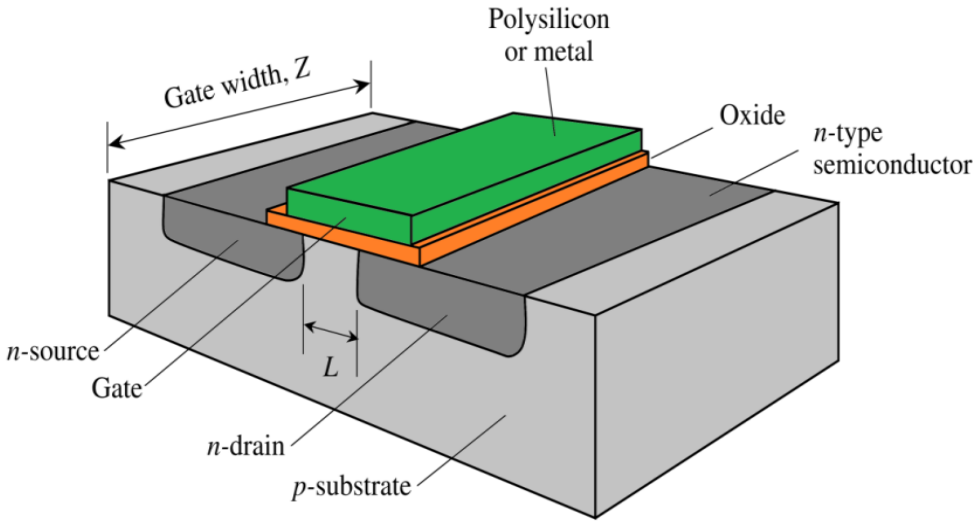
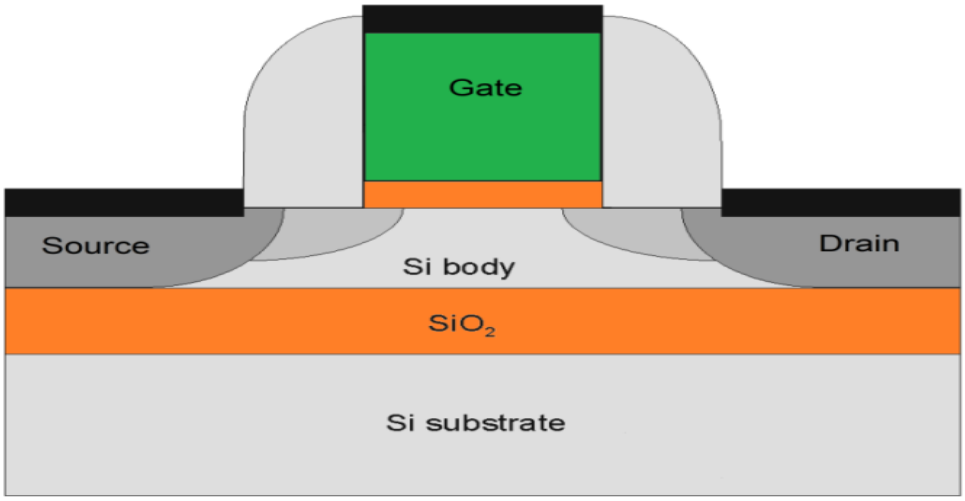


Fig I.1 Schematic of an Conventional MOS device [25]

I.2.2 Silicon on Insulator (SOI) MOSFET

It is like a conventional MOSFET but a layer of insulator (SiO_2) is added to reduces current leakage from the drain/source junction to substrate (FigI.2) [26] .The insulation layer introduces lower coupling capacitance from the conducting channel to the substrate compared to conventional MOSFET [27],[28] . It is seen that using SOI MOSFET reduces power dissipation up to 66% compared to the conventional MOSFET. And, for the same power dissipation, up to 35% improvement in operating frequency can be achieved [29]. The advantage of SOI is the ease of electrical isolation of a device from the rest of the integrated circuit, which increases packing density. Moreover, the area of source and drain junctions is significantly reduced, thus decreasing parasitic capacitances. Finally, the depletion width is limited by the Si body thickness; therefore, it is widely believed that SOI helps reduce short channel effects unless source-to-drain coupling through channel and BOX cannot be neglected. The properties of SOI devices are improved with the reduction of body thickness. It is believed that fully depleted ultra-thin-body SOI (FD UTB SOI) is one of the best scaling solutions. Due to excellent gate control of the channel, these devices may be undoped or very lightly doped. In this way mobility is not degraded and threshold voltage is less dependent on the fluctuations of doping concentration[30] . Another advantage of SOI is that it facilitates development of new device concepts[31].



FigI.2: Cross-section of a SOI MOSFET [32]

I.2.3 Double gate MOSFET

As the name suggests, these devices have two gates (Fig I.3) for simultaneously controlling the charge in the silicon body layer, allowing two channels for current flow. The two gates are present at the front and the back end. There is charge coupling between the front and back gate[33] .

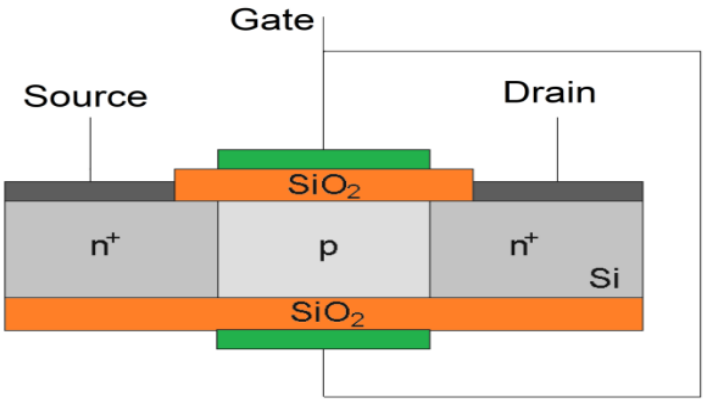
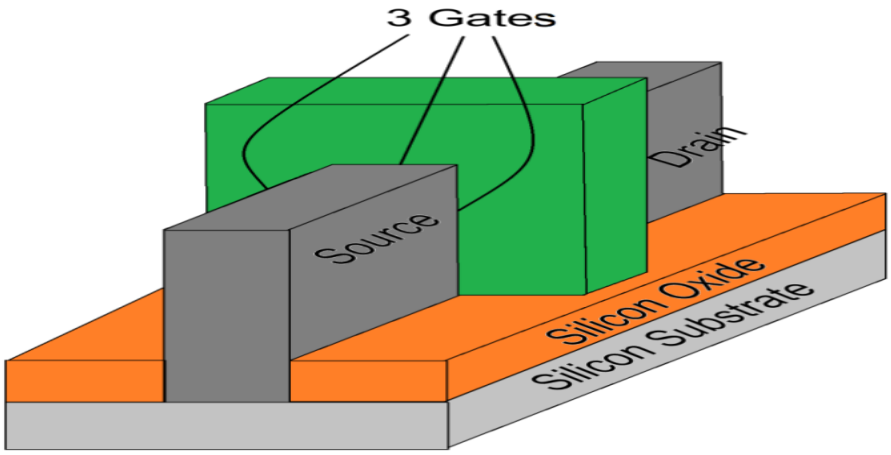


Fig I.3 Cross-section of a double gate transistor [32]

I.2.4 Multi-gate MOSFET

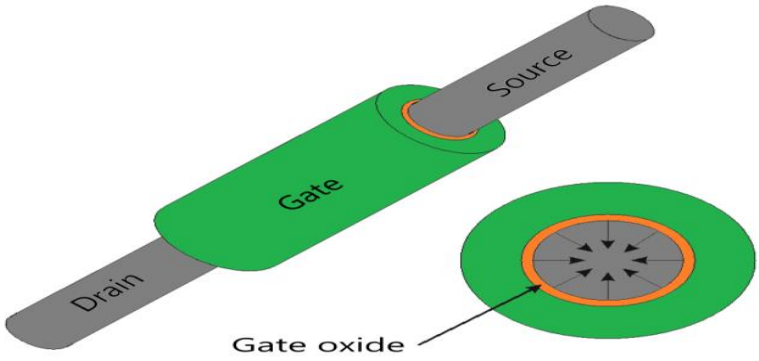
A multi-gate MOSFET or multi-gate field effect transistor (MuGFET) refers to a metal oxide semiconductor field effect transistor that has more than two gates such as three gates (FigI.4) where the increase of gates allow to control the flow of charge in the channel[34].



FigI.4 3D Tri-Gate transistor [24]

I.2.5 Surround gate MOSFET

The main problem in the above discussed devices is their control over the charge flow in the channel. So, for better control over the channel it can use surround gate MOSFET. In surround gate devices, channel is covered by gate from all sides. It is somehow similar to a FinFet. Besides providing better control over the charge flow in the channel, it also provides better accuracy[34]. Basic structure of surround gate can be shown as in FigI.5.



FigI.5 Ultimate surrounding gate MOSFET [32]

I.2.6 Silicon material properties

The most commonly used materials in electronic industries are semiconductor materials .In the past few years, Silicon (Si) was the most used semiconductor for microelectronics devices. However, Si-based devices are reaching their material limits due to the miniaturization[17]. TableI.1 gives some properties of Silicon.

TableI.1: Some properties of Silicon [17, 35]

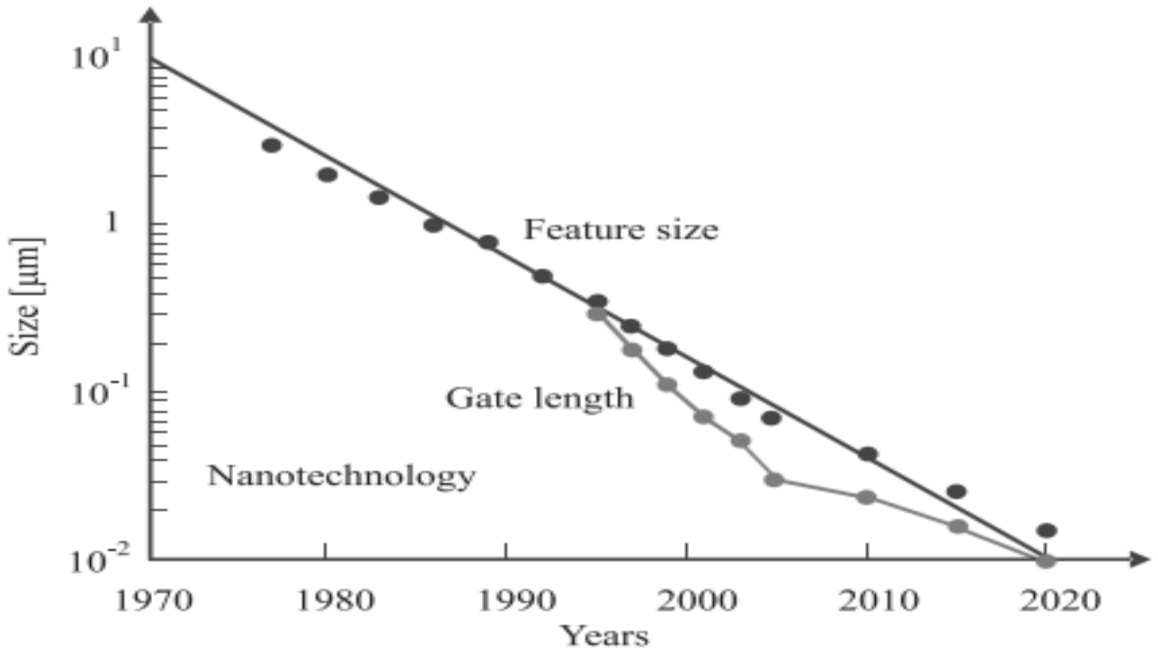
Property	Value
Thermal conductivity	150 $W.m^{-1}.K^{-1}$
Mean Free Path (MFP)	100 nm
Group velocity	3000 m/s
Volumetric heat capacity	1.5E+6 $J.m^{-3}.K^{-1}$
Electron rest mass (m_e)	9.1095E-28 g
effective electron mass	0.32 m_e

density	2.33 g/cm^3
longitudinal sound speed	9.18E+5 cm/s
acoustic phonon deformation potential	9 eV
non-parabolicity factor	0.5 eV^{-1}
relative dielectric constant	11.7
vacuum dielectric constant	8.85E-18 C/V µm

I.2.7 The reduction of feature size

The miniaturization of electronics has reached the nano-scale and you can imagine this ,with hundreds of millions of semiconductors assembled on a chip area no larger than a few square centimeters and the smallest lateral device feature sizes approach 10 nm [2].

Although nowadays more than 90 % of integrated circuits are manufactured in complementary MOSFET (CMOS)technology. The MOSFET has been improved countless times and it has been miniaturized beyond imagination. The reduction in feature size, as it depicted in FigI.6 , has been more or less exponential [22].



FigI.6 Feature size as a function of time [36]

I.3 Moore's law

Since the beginning of semiconductor electronics, the number of transistors in an integrated circuit has been doubling with time (every 18 months) [22]. This trend was first noticed by Gordon Moore [37] and is called Moore's Law. In FigI.7 the number of transistors in successive Intel processors is plotted as a function of time [38].

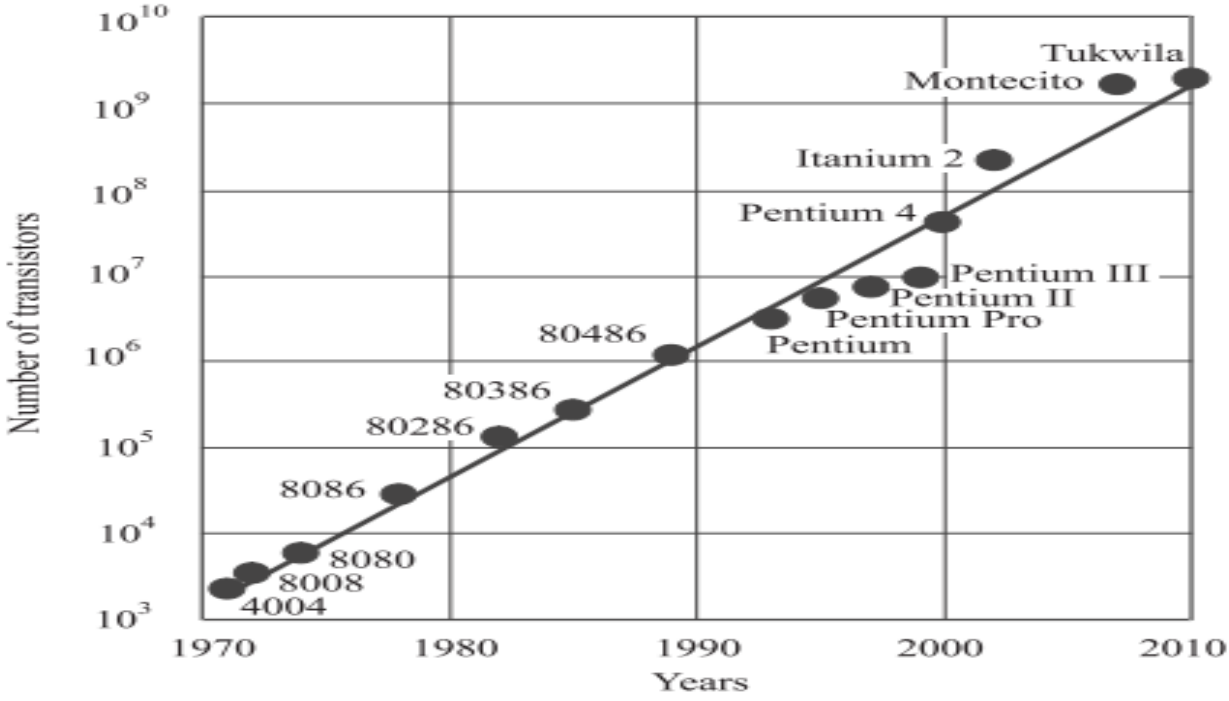


Fig I.7 :Number of transistors in successive Intel processors as a function of time [38]

I.4 Heat transport in micro / nano-structure

To treat heat transport on the micro and nanoscale, there are logically two types of methods to handle heat transport on a micro and nanoscale: theoretical and experimental [39]. The theoretical methods are divided into: macroscopic, mesoscopic and microscopic.

All of these methods are summarized in Fig I.8. Microscopic method provides atomic-scale information, while mesoscopic method produces statistical information (the particle distribution function), and macroscopic method uses only several state variables for continuum media[39].

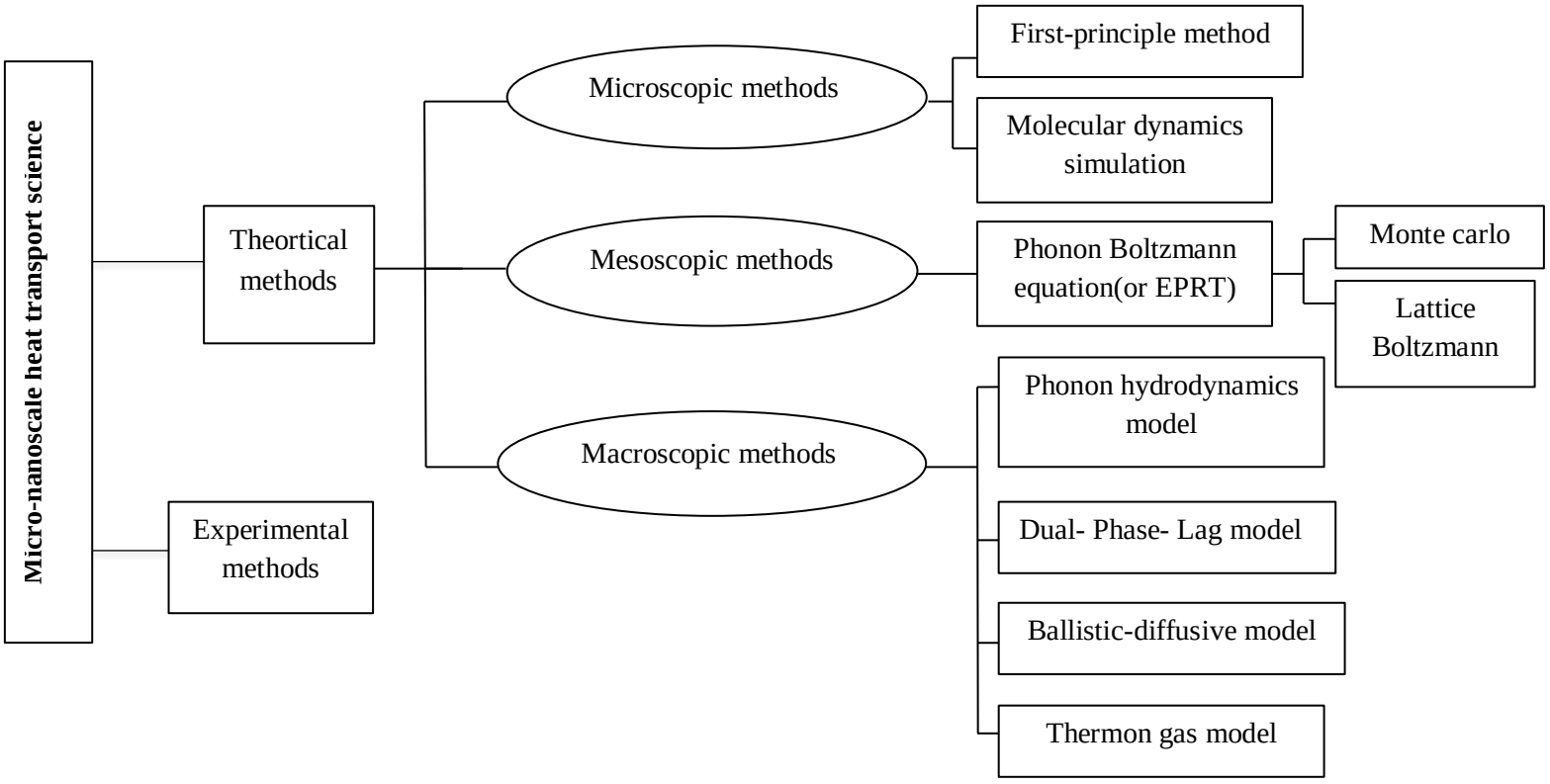


Fig I.8:Current methods in micro- and nanoscale heat transport science[39]

Cattaneo and Vernotti [40, 41] independently suggested a new model derived from the Fourier law, named single-phase lag (SPL). This equation adds a time delay between the heat flux and the temperature gradient and is called relaxation time due to the heat flux vector happening later than the temperature gradient. Tzou [42] proposed a new model for thermal transfer in nanostructure presented by the dual phase lag (DPL) where the temperature gradient may undergo the vector of heat flux, or the heat flux vector can precede the temperature gradient. Chen [43] presents another non-Fourier heat transfer model called ballistic diffusive equation (BDE). This model was derived from the Boltzmann transport equation (BTE). The researcher states that the BDE model is a good estimation of the thermal transport within the nano-

materials. Zhang et al. [44] investigated the temperature distribution in a multi-layered silicon-on-insulator (SOI) MOSFETs structure using a 2D MEDICI simulator. The results showed that the new SOI structure can eliminate the self-heating effect successfully, and can substitute the conventional buried dioxide SOI. Yang et al. [4] used a ballistic-diffusive heat conduction equation (BDE) to study two-dimensional thermal transport in a MOSFET device. Their findings were consistent with the results of the classical Boltzmann equation. Ghazanfarian and Abbassi [45] studied the heat transport in a simplified MOSFET by employing the DPL method with a temperature jump boundary condition (TJBC). A good agreement between the numerical and analytical results was reported. In addition, they reported that incorporating the proposed temperature boundary condition type into the DPL method has the potential to precisely predict the 2-D results. Nasri et al. [46] used the DPL equation to investigate the thermal behavior within a nanoscale MOS transistor device with a temperature jump condition of type. The researchers have demonstrated that the semiconductor-oxide layer collisions at the interface increase by the application of the temperature jump condition, which leads to an increase of hotspots in the nano-device. Sinha et al. [47] introduced a new phonon transport method for the non-equilibrium phonon distributions in nanoscale silicon devices with the size around 100 nm. They handled the isotropic dispersion through all phonon branches and presented a phonon emission spectrum electron-phonon scattering from independent non-Fourier Monte Carlo simulation.

A theoretical method utilizing the Boltzmann transport equation has been developed by Xu and Liqiu [48]. In another study, Xu and Li [49] suggested an analytical BTE model for describing the heat transfer in a MOSFET device. Chen and Weng [50] have numerically and analytically displayed a slip condition and jump model based on the Beskok–Karniadakis slip law and noticed that the condition had a significant role in the developing region of a micro-channel. Barletta and Zanchini [51] used the CV model to numerically study the compatibility of hyperbolic heat transport with the local equilibrium hypothesis. Sverdrup et al. [52] analyzed the heat transport in the silicon region of a silicon-on-insulator (SOI) transistor using 2D phonon Boltzmann transport equation (BTE). They found that the predicted peak temperature is almost 160% higher than the prediction using Fourier's law. Rezgui et al.[53] proposed a ballistic-diffusive equation to analyze nano-heat transfer in MOSFETs. Their study showed that when the Knudsen number is increased, the effective thermal conductivity reduces. The results of this study are in good accordance with those obtained by the BTE. Belmabrouk et al. [54]

investigated the thermal boundary resistance impact on thermal transport utilizing the BDE model and Cattaneo-Vernotte model, and reported that the heat conduction at the interfaces can be enhanced by decreasing thermal boundary resistance. A study [55] investigating the ballistic-diffusive phonon transport along Germanium/Silicon interface reported that the temperature jump happens in the interface because of phonon-wall interactions and the surface roughness effects on the interfacial thermal transfer. Analysis of the electro thermal transport involved in FinFET device was carried out by Rezgui et al.[56]. Under a more intensified electric field, the electron movement reduced and high dielectric constant oxide and minimized thermal resistance at the interface could optimize the nano-thermal behavior in the device.

To reduce the heat generated in the transistor device, other designs have been proposed. Jiang et al.[57] suggested an approach for estimation of the junction temperature of SiC MOSFET based on the dynamic threshold voltage. Though double-pulse tests, they experimentally evaluated the proposed dynamic threshold voltage calculation circuit and indicated that the dynamic threshold voltage of the SiC transistor varies linearly with junction temperature. Belkhiria et al. [58] proposed to use the high dielectric constant oxide materials in the partially insulated transistor structure. The authors found that a significant reduction in temperature rise is achieved during high power operation and utilization of Al2O3 layer can reduce the self-heating in partially insulated transistor. Ghasemi and Mozaffar [59] developed a novel SOI transistor which was able to fully remove heat by proposed scheme T-shaped 4H-SiC region established in the buried oxide layer. This new design could absorb heat from the channel active and transport it to the substrate zone, and had characteristics of higher direct current transconductance, less delay time, and higher cut-off frequency compared to traditional SOI devices.The zero-band graphene distance decreases the on-off current ratio by 2–20, rendering the wide area of graphene to an unsuitable applicant for MOS transistor system. Shrinking the one-dimensional graphene layer and creating graphene nano-ribbons can increase the current ratio. Although the thermal property of graphene layer ribbon is reducing, there are several proposals for the applications of this nano-material for the evolution of a modern generation of microelectronics technology [60, 61]. Subrina et al. [62] employed COMSOL Multi-physics software to study the heat transfer in circuits of silicon-on-insulator (SOI). The analysis was done for both including and excluding lateral heat spreaders of graphene. They depicted that the

temperature of the localized hot spots can be reduced significantly by utilization of graphene or graphene layers with proper heat sink.

I.5 Conclusion

This chapter introduces the main concepts about MOSFET systems, explaining their structure and importance. We also saw the tremendous development in reducing its size in a short period until it became invisible to the human eye, and the traditional equations for studying the thermal and electrical behavior of these devices became insufficient. Therefore, more equations models must be used to study these nano-systems.

Chapter II: Lattice Boltzmann Method

II.1 Introduction

Classically, a heat transfer problem is solved using the differential equations partial (EDP) that govern it, like the Fourier' law equation. Most traditional resolution methods (finite element method: FEM, finite differences method: FDM, finite volume method: FVM) in CFD are based on the resolution, differential or integral forms of the differential equations partial. These methods are based on discretization techniques. EDPs are derived and discretized by finite elements, finite differences or finite volumes usually in regular meshes. The resulting approximate solutions are therefore based on spatial and temporal discretization scales.

A numerical methods, alternatives to classical methods have been developed. These all tend to circumvent the difficulties linked to networking in constructing some or all of the approximation by other approaches than the spatial discretization by elements. Among these methods are the methods called non-mesh methods. These techniques have proved their effectiveness in the treatment of delicate problems to be addressed by conventional methods. Moreover, it is interesting to note that the methodological and / or mathematical concepts used in these very open approaches offer new perspectives for the numerical simulation of the complex phenomena. Among the alternative numerical methods, we find the Boltzmann method on a network which is of great interest for the improvement of the study of complex geometries, this method is completely different from traditional methods as the concept of continuity is abandoned. The main idea of Boltzmann is to bridge the gap between micro and macro approaches by not considering each particle behavior alone but the behavior of a collection of particles as a unit, this approach is called mesoscopic method.

II.2 Theory

The Boltzmann Transport Equation (BTE) derived from Kinetic theory by Ludwig Eduard Boltzmann, this Austrian physicist whose greatest achievement was in the development of statistical mechanics. This equation considers the movement of molecules and describes their behavior statistically following a continuous function in time, velocity and space.

II.3 Phonon mechanism scattering process

A phonon is the quantum mechanical description of an elementary vibrational motion in which a lattice of atoms or molecules oscillates. The phonons play a major role in many of the physical properties of material, such as thermal conductivity. The phonons scattering processes tend to

change some of the properties of phonons depending upon the type of scattering process they undergo. Some of the common scattering processes that a phonon undergoes are[63]:

 Impurity scattering: They are mainly due to the impurities in a crystal, crystal imperfections, defects in a crystal structure etc.

 Phonon-phonon scattering: These scattering events occur when two phonons collide while drifting from one point to another in a domain.

 Phonon-electron scattering: When a phonon collides with an electron, phonon electron scatterings take place.

 Interface scattering: These scattering events are due to a foreign material incorporated into a host material as an interface.

 Boundary scattering: Boundary scatterings are when a phonon encounters domain boundary. These scatterings are particularly important in the ballistic phase of phonon transport as the domain size is very small and the phonons encounter the boundaries many times during their lifetime.

II.4 Phonon Boltzmann transport equation

Phonons, which are quanta of lattice vibrations, are the primary thermal energy carriers in semiconductor materials. The thermal properties of semiconductor materials are determined by the propagation and collision of phonons and the interaction of phonons with other carriers. In this work, the BTE, which accounts for the phonons scattering, is utilized to examine the heat transfer in the nano-transistors. To include the heat transport effect in the nanoscale devices, the transient Boltzmann transport equation for phonons is given by [64-66]:

$$\frac{\partial g}{\partial t} + v.\nabla g = \frac{g^{eq} - g}{\tau} \tag{II.1}$$

Here, g, g^{eq}, v, and τ respectively represent the phonon distribution function, equilibrium distribution function, phonon group velocity, and single relaxation time associated to resistive collisions of the phonons given by [67, 68]:

$$\tau = \frac{3 \times k}{C \times v^2} = \frac{\Lambda}{v} \tag{II.2}$$

where k, Λ and C respectively stand for the thermal conductivity, the mean free path, and volumetric heat capacity. The equilibrium distribution function described with the Bose–Einstein model for phonons is given as follows [19, 69]:

$$g^{eq} = \frac{1}{e^{(\hbar\omega/k_B T)} - 1} \tag{II.3}$$

In the above equation, $\hbar$ and k_B are respectively the reduced Planck's and Boltzmann constants, whereas ω and T represent the phonon frequency and absolute temperature. The heat flux is calculated by Eq.(II.4) [48]:

$$q = \sum_p \int v g \hbar \omega_p D_p(\omega) d\omega \tag{II.4}$$

where p and D_p respectively denote the polarization of phonons and phonon state density function.

For convenience, Eq. (II.1) can be cast into the phonon energy density BTE as follows [70, 71]:

$$\frac{\partial u}{\partial t} + v.\nabla u = -\frac{u - u^{eq}}{\tau} + q_v \tag{II.5}$$

This formula is also known as the quantum mechanical equation for phonons, where q_v is the volumetric heat generation.

An alternative definition of temperature, assuming that the total phonon energy in a given lattice point is identical to the phonon energy at the corresponding temperature, is proposed. By that, the phonon energy and temperature is linked via the Debye model [19, 72-74]:

$$u(T) = \left(\frac{9\eta k_B}{\theta_D^3} \int_0^{\theta_D/T} \frac{z^3}{e^z - 1} dz \right) T^4 \tag{II.6}$$

Here θ_D ,η and z respectively stand for the Debye temperature, number density of oscillators, and dimensionless variable.

II.5 Lattice Boltzmann methodology

Lattice Boltzmann method is an effective technique for solving the Boltzmann transport equation. This method has attracted considerable attention in recent years due to offering considerable advantages for resolving the boundaries, successfully handling the multi-scale coupling problem, and allowing easy programing. The single-mode LBM for phonon transportation is considered a solution of the BTE to estimate the distribution function of a representative phonon mode. As only one representative mode with mean phonon properties is regarded in the single mode approximation, all phonons are deemed to have the same relaxation time and velocity [75]. Since the objective of this study is to address the thermal behavior of nano-scale transistors using the LBM for nano-heat transport, the single-mode LBM was adopted for simplicity and clarification purposes. The LBM discretes the space domain by defining the lattice positions. During the LBM simulation, at each time step the distribution functions shift towards the assigned discrete velocity set to the next lattice site, and on the basis of a set of collision principles, new distributions are determined for the next step at each lattice site [69, 76]. The derivative terms in Eq. (II.5) can be discretized as follows:

$$\frac{\partial u}{\partial t} = \frac{u(\mathrm{x}, t+\Delta t) - u(\mathrm{x}, \mathrm{t})}{\Delta t} \tag{II.7}$$

$$\frac{\partial u}{\partial \mathrm{x}} = \frac{u(\mathrm{x}+\Delta \mathrm{x}, t+\Delta t) - u(\mathrm{x}, \mathrm{t}+\Delta t)}{\Delta \mathrm{x}} \tag{II.8}$$

Eqs.(II.7)-(II.8) are associated with the discrete phonon energy distribution functions. Then the discretization of Eq. (II.5) is given by [70, 71]:

$$\frac{u_i(\mathrm{x}, t+\Delta t) - u_i(\mathrm{x}, \mathrm{t})}{\Delta t} + c_i \frac{u_i(\mathrm{x}+\Delta \mathrm{x}, t+\Delta t) - u_i(\mathrm{x}, \mathrm{t}+\Delta t)}{\Delta \mathrm{x}} = -\frac{u_i(\mathrm{x}, t) - u_i^{eq}(\mathrm{x}, \mathrm{t})}{\tau} + w_i q_v \tag{II.9}$$

where x is the position vector, t is the time, c_i is the discrete velocity, Δt is the time step and Δx is the space step while w_i denotes the weighting factor for each direction. .

The time step and lattice space step can be made by $\Delta \mathrm{x} = c_i \Delta t$. This leads to an LBM with an internal heat generation , Eq. (II.9) can rewritten as:

$$u_i(\mathrm{x}+\Delta \mathrm{x}, t+\Delta t) - u_i(\mathrm{x}, \mathrm{t}) = -\frac{\Delta t}{\tau}\left[u_i(\mathrm{x}, t) - u_i^{eq}(\mathrm{x}, \mathrm{t})\right] + \Delta t w_i q_v \tag{II.10}$$

The expression $u_i(x,t)$ is related to the independent energy density of the phonon which is proportional to the phonon population linked with a particular position in the lattice. The overall energy density of phonons can be calculated by summing the discrete energy densities of phonons across all directions of the lattices [70]:

$$u(\mathrm{x},t)=\sum_{i=1}^{d}u_i(\mathrm{x},t)=\sum_{i=1}^{d}u^{eq}(\mathrm{x},t) \tag{II.11}$$

The equilibrium phonon energy density can be calculated by Eq. (II.11) assuming that it is the same in all lattice directions:

$$u_i^{eq}(\mathrm{x},t)=\frac{u(\mathrm{x},t)}{d} \tag{II.12}$$

II.6 Lattice arrangements

The common terminology used in LBM is to refer to the dimension of the problem and the number of speed is using D_nQ_m, where n represent the dimension of the problem (1 for 1-D, 2 for 2-D and 3 for 3-D) and m refers to the speed model, number of linkages[77].

II.6.1 One-Dimensional

Fig II.1 illustrates the lattice used for the description of the model D_1Q_3 and D_1Q_2

Fig II.1 : Lattice arrangements for 1-D problems

For D_1Q_3 ,the discrete velocity set is given by:

$$\{c_0=(0,0)c, c_1=(1,0)c, c_2=(0,-1)c\} \tag{II.13}$$

We speak of the model D_1Q_2 when the particle (0) at rest is not considered. discrete velocity is presented as:

$$\{c_1=(1,0)c, c_2=(0,-1)c\} \tag{II.14}$$

II.6.2 Two-Dimensional

Fig II.2 shows the D_2Q_9 model and the discrete velocity set is:

$$\left\{\begin{array}{l} c_0=(0,0)c, c_1=(1,0)c, c_2=(0,1)c, c_3=(-1,0)c, c_4=(0,-1)c, \\ c_5=(1,1)c, c_6=(-1,1)c, c_7=(-1,-1)c, c_8=(1,-1)c \end{array}\right\} \quad \text{(II.15)}$$

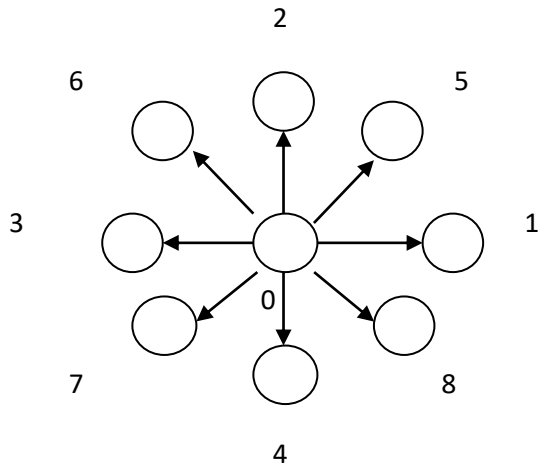


Fig II.2: Lattice model D_2Q_9

Fig II.3 shows the D_2Q_5 model and the discrete velocity set is:

$$\left\{c_0=(0,0)c, c_1=(1,0)c, c_2=(0,1)c, c_3=(-1,0)c, c_4=(0,-1)c,\right\} \quad \text{(II.16)}$$

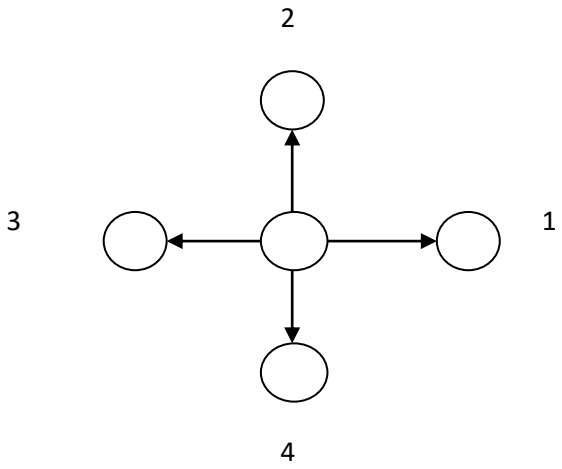


Fig II.3: Lattice model D_2Q_5

II.6.2 Three-Dimensional

In general two models are used in simulation of three dimensional problems,D_3Q_{15} and D_3Q_{19}

$$c_i \begin{cases} (0,0,0)\,\mathrm{c} & \mathrm{i} = 0 \\ (\pm 1,0,0)\,\mathrm{c}, (0,\pm 1,0)\,\mathrm{c}, (0,0,\pm 1)\,\mathrm{c} & \mathrm{i} = 1..6 \\ (\pm 1,\pm 1,0)\,\mathrm{c}, (\pm 1,0,\pm 1)\,\mathrm{c}, (0,\pm 1,\pm 1)\,\mathrm{c} & \mathrm{i} = 7..18 \end{cases} \qquad \text{(II.17)}$$

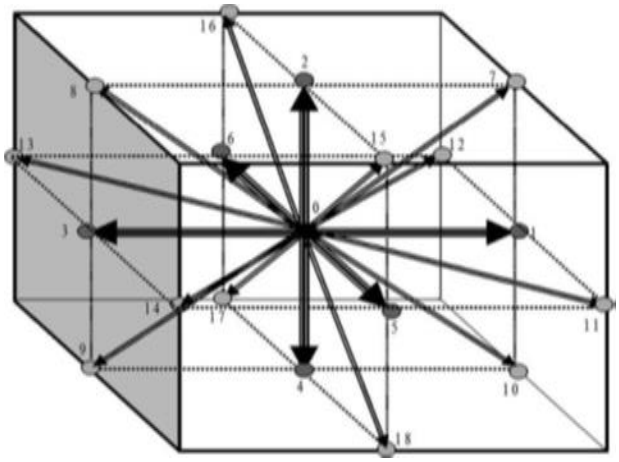


Fig II.4: Lattice arrangements for 3D problems, D_3Q_{19}

$$c_i \begin{cases} (0,0,0)\,\mathrm{c} & \mathrm{i} = 0 \\ (\pm 1,0,0)\,\mathrm{c}, (0,\pm 1,0)\,\mathrm{c}, (0,0,\pm 1)\,\mathrm{c} & \mathrm{i} = 1..6 \\ (\pm 1,\pm 1,\pm 1) & \mathrm{i} = 7..14 \end{cases} \qquad \text{(II.18)}$$

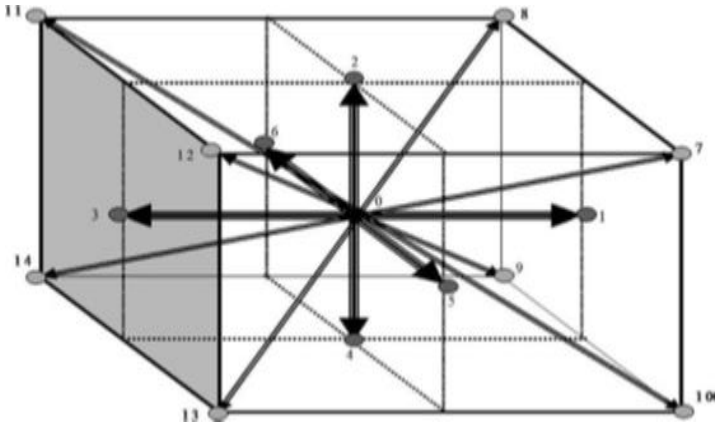


Fig II.5: Lattice arrangements for 3-D problems, D_3Q_{15}

II.7 Application of lattice Boltzmann method

The LB method has shown a great ability to simulate systems hydrodynamic, multiphase, multi-component flows, in porous medium and heat transfer [78-80]. Fig II.6 shows some areas of application of the LB method.

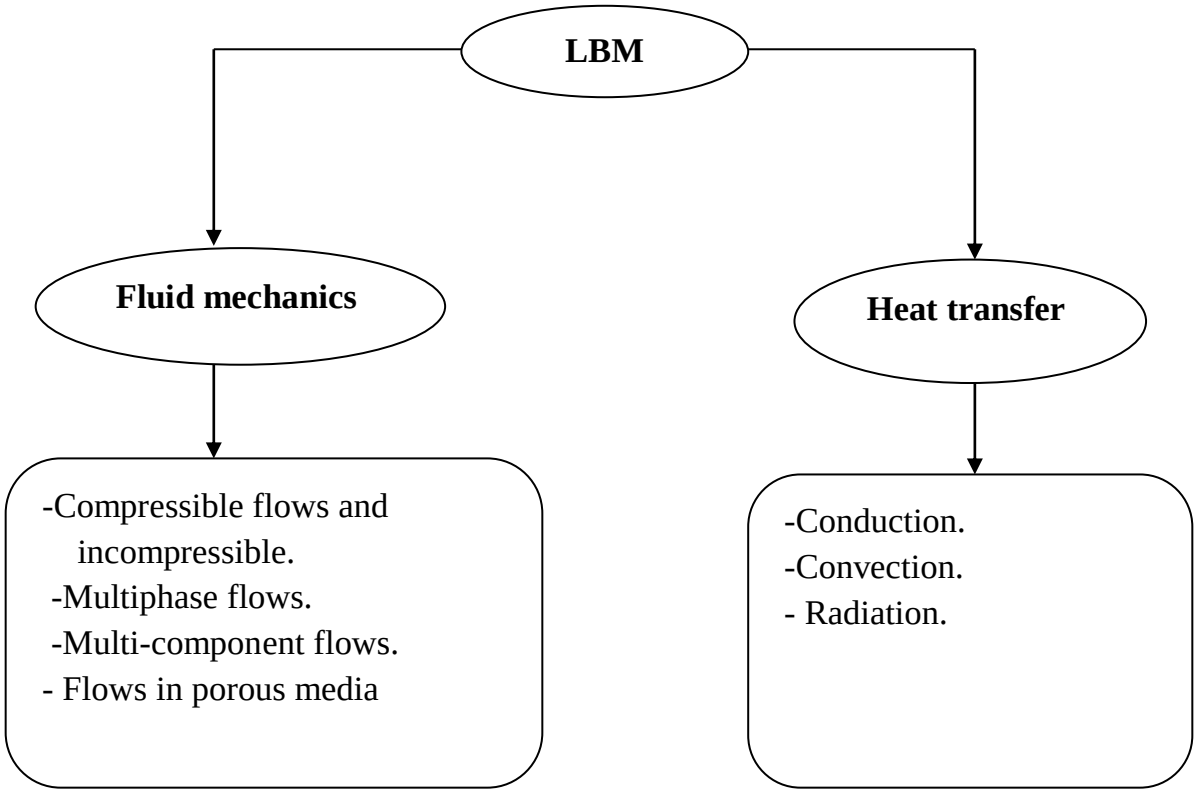


Fig II. 6: Different areas of application LBM

II.8 About the code

The simulation of the heat transfer described in this work was performed using an adopted lattice Boltzmann method implemented in the Fortran programming language. The common features of LBM, collision, scattering, the different boundary conditions are applied, and values variables are calculated. The developed informatics is presented in Fig II.7. The code has the ability to write the values in data format. To visualize the results, Tecplot software is used to read and plot the output data files.

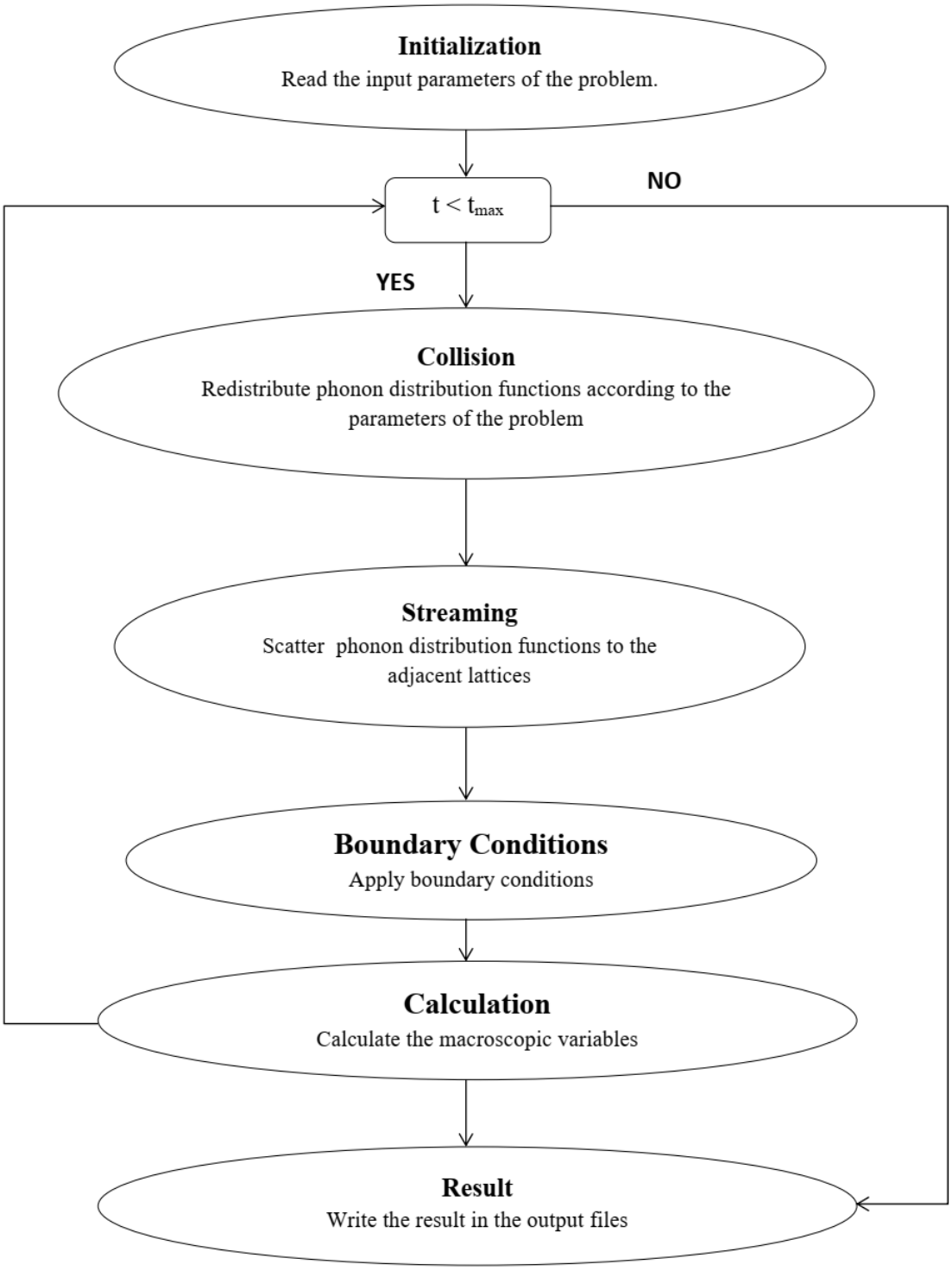


Fig II.7: Informatics organigram of LBM code

II.9 Conclusion

Numerical simulation by alternative methods is the subject of numerous research work in the world. When implementing these methods, the heat transfer and structure domains are no longer represented by a mesh, but by a set of control points representing elementary volumes of matter that are tracked in their movement. For many years, the lattice Boltzmann method (LBM) has been applied successfully to simulate fluid flows and transport phenomena. Unlike conventional methods like CFD.

Chapter III: Analysis of Thermal Behavior in MOSFET devices

III.1 Introduction

From the first appearance of semiconductor electronics to today, the number of transistors integrated in a circuit has been increasing about two folds for every 18 months [22, 37]. In present integrated circuits, the feature size of electronic devices is comparable or even less than the mean free path of the phonon on which the transistors are built [1-4]. MOS transistors were influenced by this miniaturization and the MOSFET channel region has become smaller than the phonon mean free path [5]. To analyze the efficiency of integrated circuits consisting of transistors, the study of thermal transfer within the nano MOSFET is very important to demonstrate the thermal stability of the devices and its efficiency [6, 7]. In ultra-small semiconductor devices, the heat generated by the Joule effect can be very high as the operation power of the device cannot be reduced under a certain value [5]. Moreover, switching time of MOSFET devices reaches the phonon relaxation time, which is less than 100 ps in silicon[4, 8-10]. It is well-known that micro-nano scale heat transfer can be considerably different from Fourier's law because of the limited relaxation time of heat carriers [11]. The Boltzmann transport equation (BTE) and Monte Carlo (MC) simulation are applied to investigate the thermal transfer mechanism in structures from meso to macro-scale ,where the meso-scale method produces statistical information (the particle distribution function) in sub-continuum medium due to the movement of particle (vibration) and then we find macro-scale variable physic by collecting the functional distributions [12-14]. The present work has the aim to perform a comparative analysis in terms of thermal stability between a 2D traditional MOS transistor and SOI transistor utilizing lattice Boltzmann model employed with the boundary condition of temperature jump. The considered model was compared with the simulation data retrieved from previous studies [4, 9, 16, 68].

III.2 Problems description

SOI-MOSFET is a type of transistor that utilizes an electric field in order to control the flow of current. These systems are devices having three terminals: i) source through which electrons enter the channel, ii) gate which controls the current flow through the channel and iii) drain through which the inlet electrons leave.

Despite the researches on materials used in the electronics industry, silicon remains the most widely used element in manufacturing of MOS transistors technologies, because of its presence

in nature [9, 16, 22, 81]. Recently, some chip manufacturers have begun to utilize a chemical compound of silicon and germanium in MOSFET channels. In order to produce either a p-type or an n-type semiconductor, the transistor channel is doped. The drain and source may be doped of opposite type to the channel. Since data on developing MOS nano-devices in terms of sizes, materials, and experimental results are not publicly available because of the competition between manufacturers, this data is blocked, and the relevant information was collected from previous literature works [4, 8, 9, 16, 53, 68]. For the study suggested by the mesoscopic method, the simulation designs are portrayed in Figs III.1 and III. 2. Fig III.1 shows the structure of a traditional MOS transistor device while Fig III.2 displays the structure of an SOI-MOS transistor. The sizes of devices considered in this work are L=100 nm, l =50 nm and depth of transistors is W=1 μm with a heat generation area of Lc×10 nm while d_{ox}=10 nm, where d_{ox} denotes the buried dioxide silicon thickness of SOI device. The volumetric heat source in a channel area of nano transistors is assumed to be constant (q_v=10^{19} W/m^3).

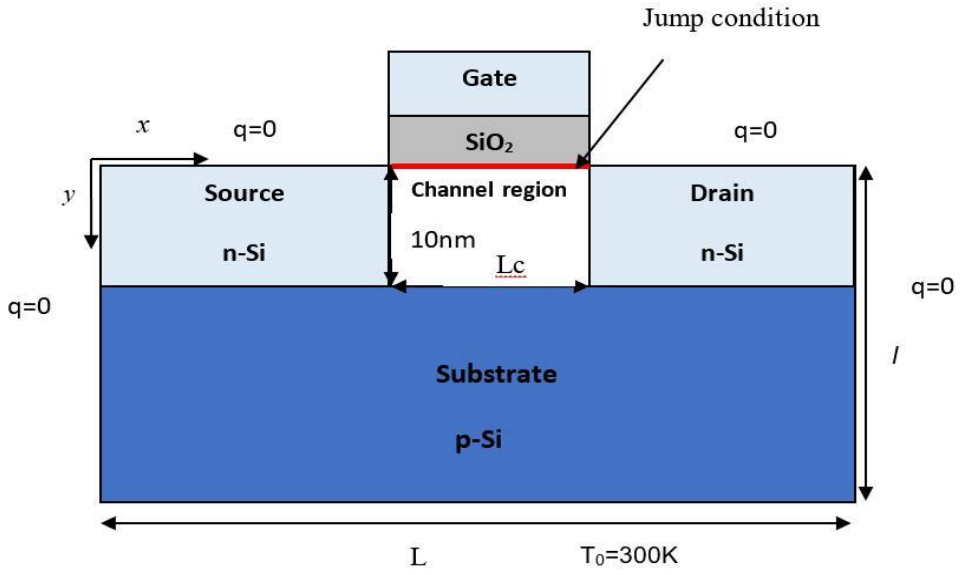


Fig III. 1 A schematic representation of traditional MOSFET

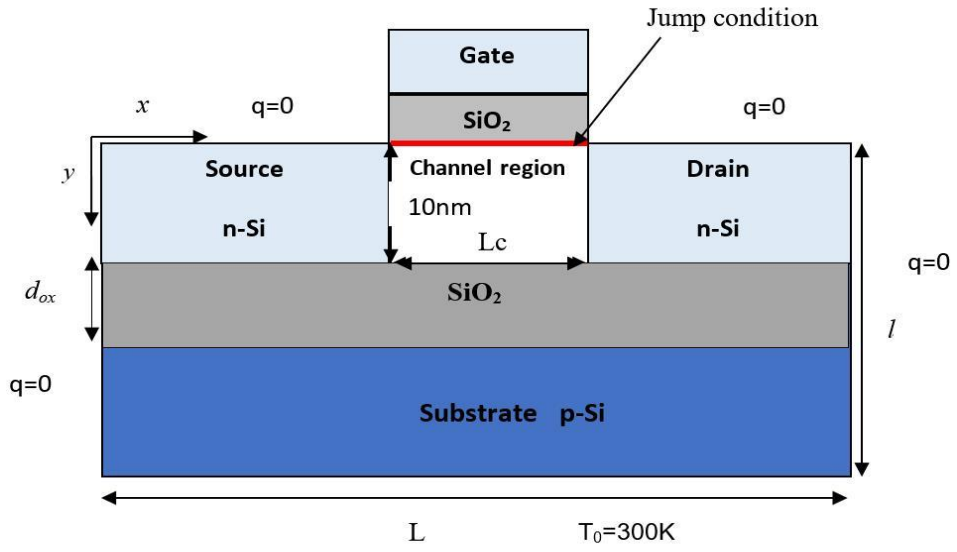


Fig III. 2. A schematic representation of SOI-MOSFET

Since the phonon traveling length 30 nm in 10 ps is much shorter than the length of third direction (W=1 μm), the heat transfer can be considered in a two-dimensional space [4, 16]. The simulation results are represented at t=30 ps.

III.3 Boundary conditions

The top, right, and left boundaries in both nanoscale transistors are assumed adiabatic, whereas at the bottom boundary is supposed to be isothermal. A constant heat source in the channel region is considered and the initial temperature of nanodevices is preserved at 300 K. The phonons scattering processes tend to change some of the properties of phonons depending upon the type of scattering process they undergo. In the present state, the transmission events are due to a foreign material incorporated into a host material as an interface. This phenomenon is taken into consideration by a temperature jump boundary condition.

The parameters defined below are implemented for non-dimensionalization:

$$u^* = \frac{u - u_{ref}}{u_{ref}}, x^* = \frac{x}{\Delta x}, y^* = \frac{y}{\Delta y}, t^* = \frac{t}{\Delta t}, T^* = \frac{T - T_{ref}}{T_{ref}}, q_v^* = \frac{\Delta t \times q_v}{C \times T_{ref}} \qquad \text{(III.1)}$$

Here, *ref* and * respectively denote reference parameters and dimensionless parameters.

At the semiconductor-oxide interface, the temperature jump boundary condition is related to oxide-gate [9, 16]. As aforementioned, this boundary condition defines transistor wall-phonon collisions and is described as follows [65, 66, 82]:

$$T^* - T_w^* = -a \times Kn \times L_c^* \frac{\partial T^*}{\partial y^*} \tag{III.2}$$

where, T_w^* denotes the dimensionless temperature of wall, and a presents an adjustable coefficient defined as [8]:

$$a = \sqrt{0.0037 + 0.4022 e^{-Kn}} \tag{III.3}$$

Several models of Lattice Boltzmann method have been proposed for simulation of heat transfer phenomenon[70, 75], among which the D_2Q_8 can provide a reasonable accuracy for high Knudsen numbers [10, 83, 84]. The lattice for D_2Q_8 model shown in Fig III.3 describes discrete points structured in a regular mesh. In this model, D_2 denotes spatial dimensions, and Q_8 indicates a direction speed connecting on each lattice site.

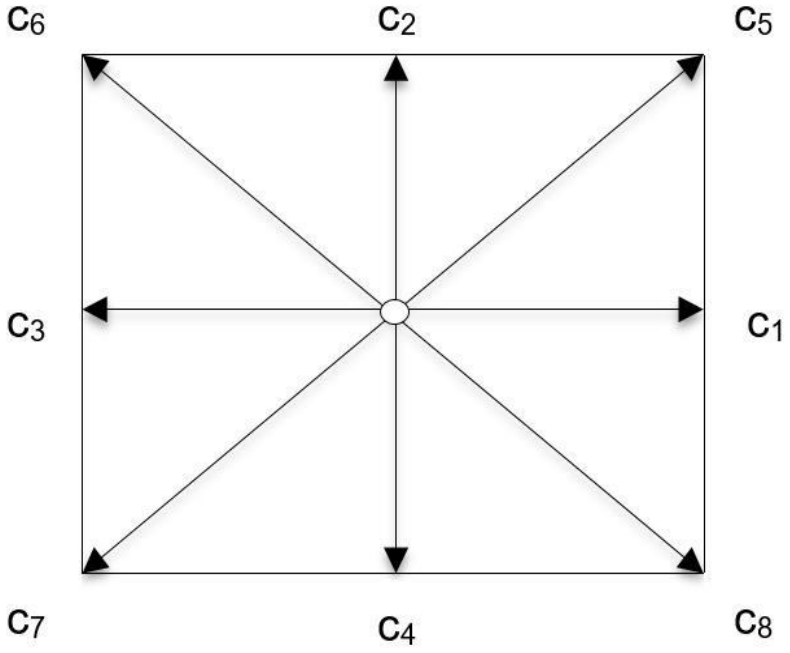


Fig III.3. A schematic for D_2Q_8 model

The time step (Δt) is 0.05 ps and the lattice space steps ($\Delta x = \Delta y$) in the structure are equidistant (0.1 nm). For the thermal transport, bi-dimensional simulation via the present model is suggested. At the bottom of transistors, the isothermal boundary condition is expressed as [69]:

$$u_i^*(x^*, m) = \frac{1}{8} u^*(x^*, m) \qquad i = 1..8 \tag{III.4}$$

At the right, left, and top (source-drain) boundaries, the adiabatic condition is used. It can be handled as follows:

$$\begin{aligned} &u_i^*(0, y^*) = u_i^*(1, y^*) \\ &u_i^*(n, y^*) = u_i^*(n-1, y^*) \quad i = 1..8 \\ &u_i^*(x^*, 0) = u_i^*(x^*, 1) \end{aligned} \tag{III.5}$$

The temperature jump boundary condition at the interface is handled as follows:

$$u_i^*(x^*, 0) = \frac{\frac{\Delta y^*}{L_c^*}\frac{u_w^*}{8} + a.Kn.u_i^*(x^*, 1)}{\frac{\Delta y^*}{L_c^*} + a.Kn} \qquad i = 1..8 \tag{III.6}$$

where (m), and (n) denote the lattice in x-, y-directions, (0) and (1) represent lattices on the boundary and next to the boundary respectively, whereas u^* is the dimensionless particle energy and u_w^* represents the dimensionless energy of the wall.

III.4 Mesos-scale study of heat transfer

In the current study, a 2D heat transport within nanoscale MOS transistors is documented employing the LBM model coupled with temperature jump condition type. Table III.1 lists the heat properties of dioxide silicon (SiO_2) and silicon (Si) that are needed for the numerical simulation in this study. Also, the influence of length of channel region on the heat conduction in conventional MOSFET and SOI-MOSFET is examined for Lc =10 nm (Kn=10) and Lc =20 nm (Kn=5).

Table III.1: Thermal features of Silicon (Si) and Silicon dioxide (SiO_2) [16, 68]

Material	k (W/m·K)	v (m/s)	Λ (nm)	C (J/m^{3}K)
Si	150	3000	100	1.5×10^6
SiO_2	1.4	5900	0.4	1.75×10^6

Fig III.4 compares the temperature difference ($T-T_{ref}$) at the centerline of the nano-MOSFET and SOI-MOSFET with time for *Kn* =10. The outputs of our proposed model are compared with those of the classical BTE[4], BDE[68], Fourier law[4], SPL model[9], and CV model [16]. A comparison between the obtained findings by the present LBM model and the previous studies that have used BTE, BDE, SPL model reveals a good agreement on the form of increasing peak temperature. The reason for different curves amplitude between these models and Fourier law stems from the assumption of finite heat diffusion speed in nanoscale regime due to the additional terms included in BDE, and SPL models compared with the heat transfer based on the Fourier equation [8, 18]. In addition, for the variation of heat sources applied inside the device, the Fourier law includes only the heat generated by the Joule effect, while the classical BTE considers the phonon emission and the Joule effect. However, the present model, BDE and SPL models include the volumetric heat source (Joule effect) as well as collision phonon-wall. In the SOI device, on the other hand, the curve of CV model takes the form of an exponential increase compared with our model which is saturated at *t*=15 ps. From the results of our proposed model, it is seen that the peak temperature increases in SOI transistor at *t*=10 compared with MOS transistor because of the effect of the insulation layer (SiO_2) that resists the passage of heat to the substrate where the peak temperature rise with respect to the reference case of 300 K is saturated at 32.4 K for the present model for MOS transistor and 39.6 K for SOI device. The difference between the present result and CV model in SOI-MOSFET is due to the saturation of the phonon energy in the proposed model in a short time at a small range, which leads to thermal stability. From the simulation results, it is also noted that the relative deviation difference between the present model and other models is case specific, as shown in Table III.2. For example, the minimum and maximum differences are 16.6% and 83.6% for the BTE and Fourier equation,

respectively, compared with the present model for MOSFET. These results implies that the present LBM model could give out nearly the same trends of results and amplitude in terms of peak temperature without any additional terms. In other side, the Fourier law is not capable of carrying phonons in nanodevice because the temperature gradient in this equation is much greater than that of the diffusive part.

Table III.2. Relative deviation for different models compared with the present model for *Kn*=10 in nano-MOSFET

Model / Parameter	Present LBM model	BTE	BDE	SPL	Fourier law
Temperature difference	32.4 K	27 K	21.3 K	19.5 K	5.3 K
Relative deviation	-	16.6%	34.2%	39.8%	83.6%

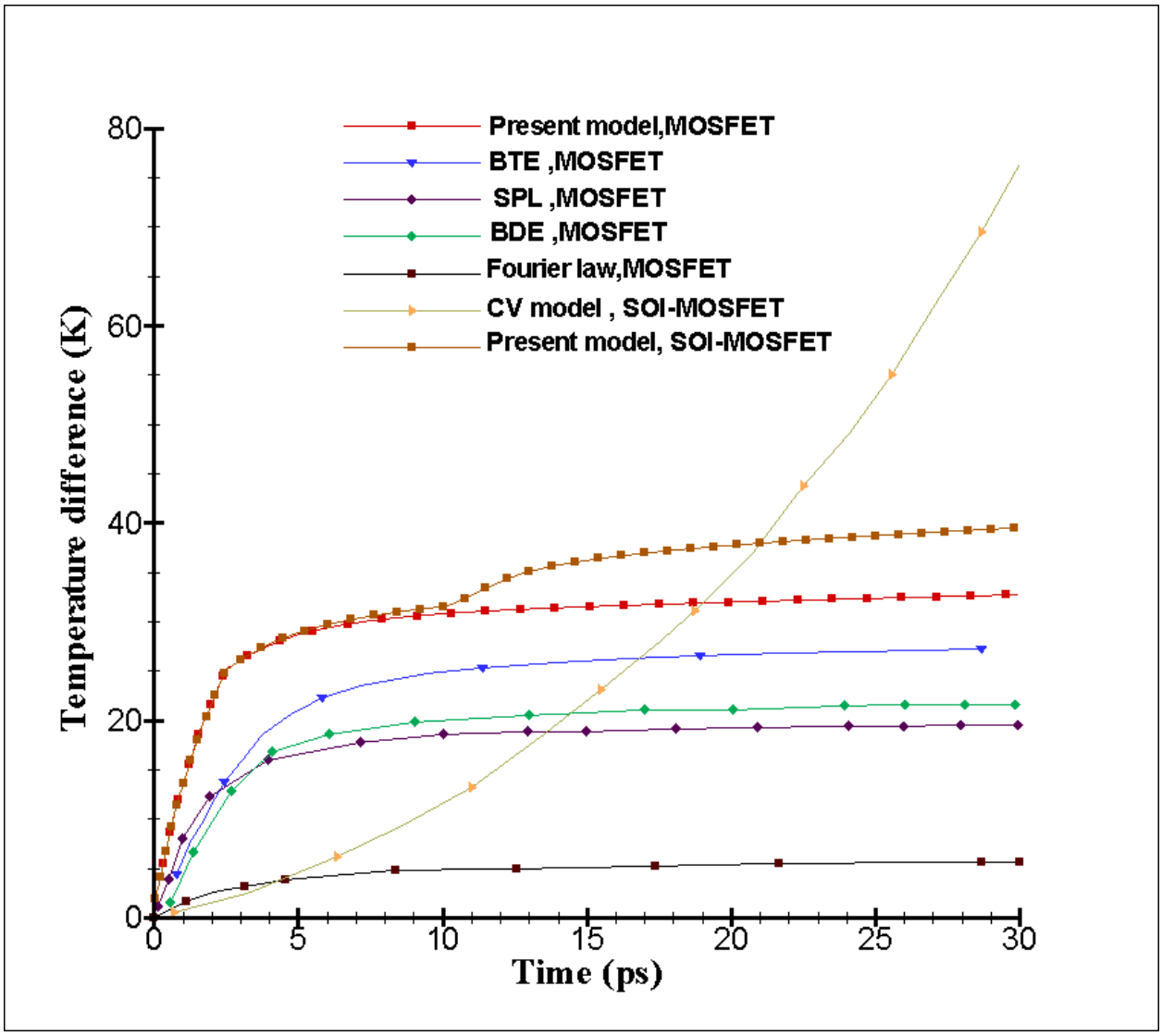


Fig III.4. Comparison of the temporal temperature difference of the conventional MOSFET and SOI-MOSFET at $x=L/2$ and $y=0$ obtained by different models

Fig III.5 displays the comparison of the temperature difference ($T-T_{ref}$) in the y-axis at the centerline of nano-transistors at time scale t=10 ps. The maximum hotspot which is found at the interface is higher than that of the previous works through other models BDE [53], SPL [9], DPL [8], and CV model [16]. Comparing the models for MOSFET, it is seen that temperatures obtained for all models start to increase from y=30 nm until reaching a maximum value in the interface between semiconductor and oxide, which is 30.5 K in the present model. In addition, it

is noticed that the SPL model and DPL model have almost the same profile plot except for the maximum temperature at Si/SiO_2. The temperature profile of present model undergoes several form changes while it reaches the maximal hotspot at the interface. The present model relies on a mesoscopic scale to describe the collision rate at the interface and the phonon heat transport while other models employed the macroscopic theoretical equations. As can be seen from the peak temperature comparison between the current model and CV model in SOI-MOSFET, the

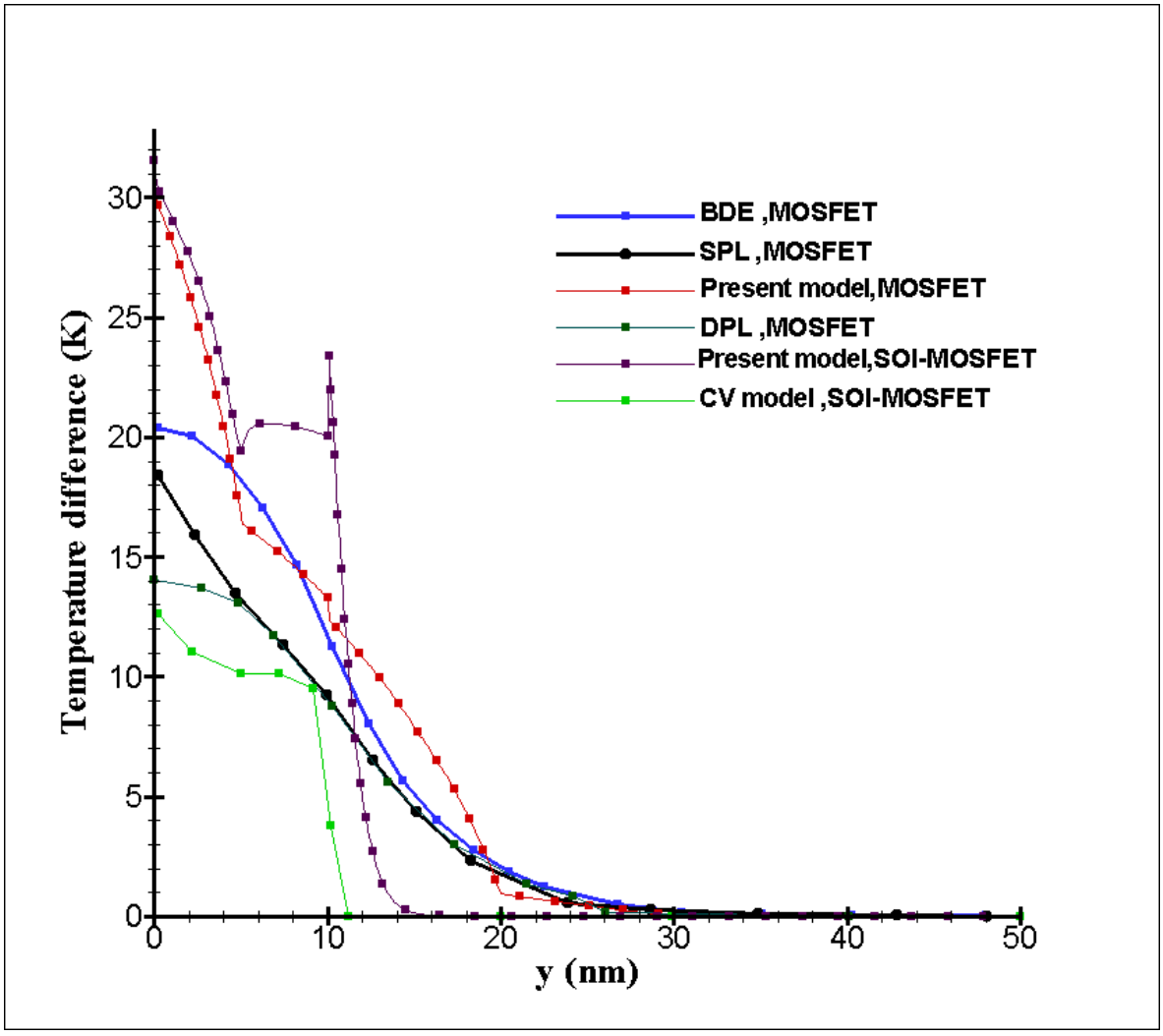


Fig III.5. Temperature difference profiles along y-direction in the centerline of the MOSFET and SOI-MOSFET with the present model, SPL, BDE, DPL and CV models at t = 10 ps

temperature reduces and then elevates to a maximum value again at y= 10 nm in the channel region due to the high thermal resistivity at the oxide zone (SiO_2). Furthermore, there is a

temperature decline in the insulation layer where the temperatures are stable in the substrate. For both devices, the maximum temperatures increase with time in the interface because of the generated heat by the Joule effect and phonon-wall collision.

Fig III.6 presents a comparison of the temperature difference ($T-T_{ref}$) along the *y*-direction at the centerline ($x=L/2$) of MOSFET and SOI-MOSFET nano-devices at t=30 ps. When the present model comes into comparison with the CV model [16] for SOI transistor, it is seen that the maximal temperature at the interface reaches 39.6 K for the present model and 80 K for the CV

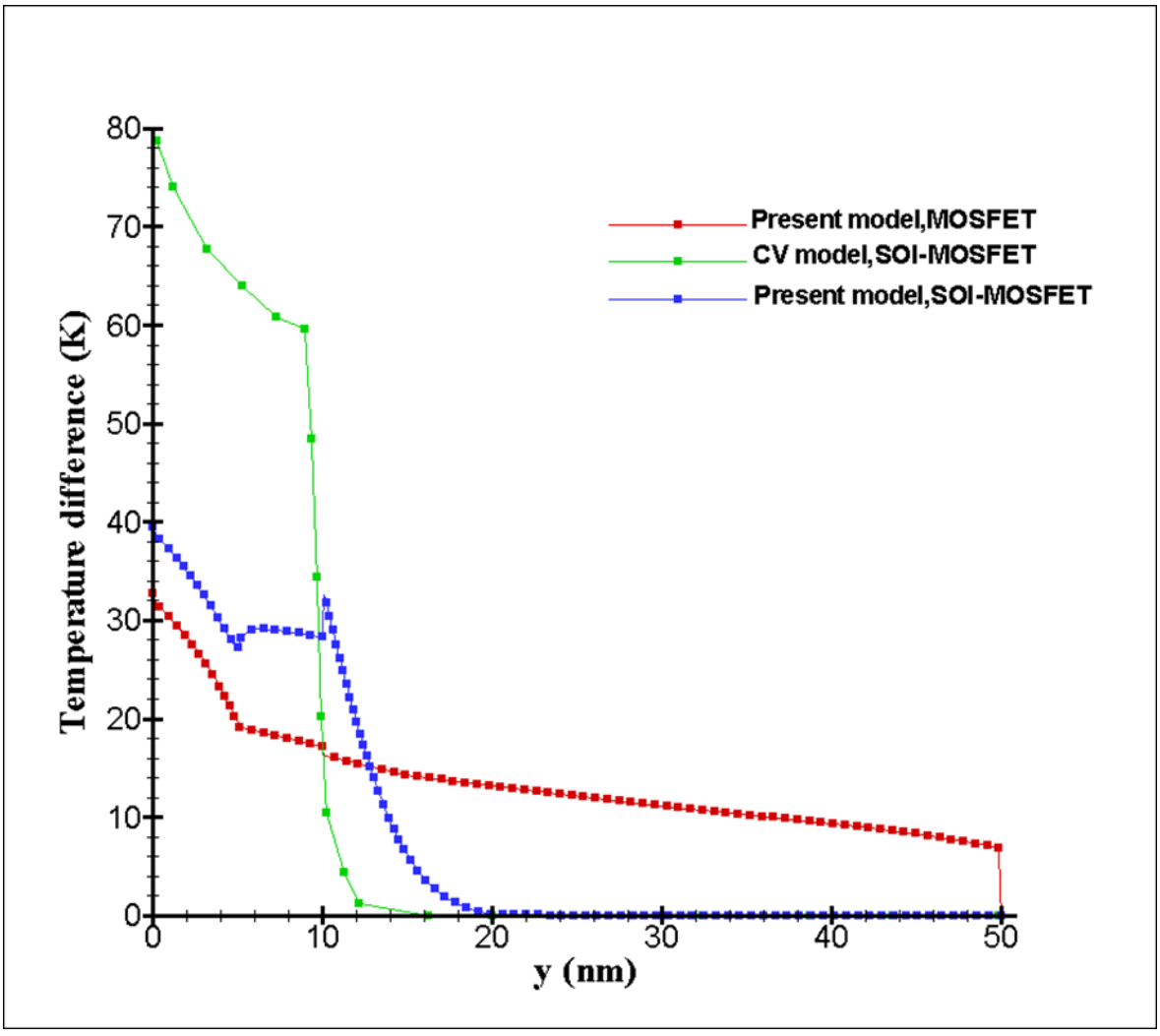
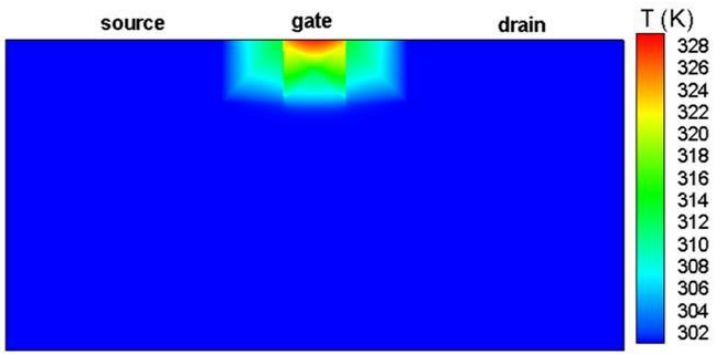


Fig III.6. Peak temperature profiles along y-direction in the centerline of the MOSFET and SOI-MOSFET with the present model and CV model at t = 30 ps.

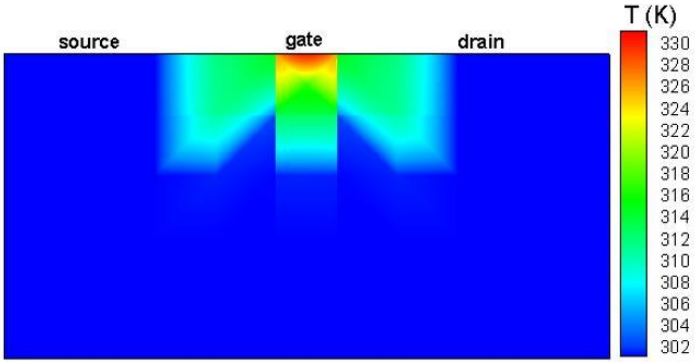
model. This difference of the maximal hotspot is caused by different models used. In addition, it can be observed that the peak temperature is estimated at 32.4 K at Si-SiO_2 interface (top

channel region of MOSFET). Furthermore, the curve of temperature has a sharp decline at the bottom of MOS transistor due to heat diffusion (collision phonon-wall and Joule effect) in a space less than the mean free path of silicon. The SiO_2 layer between the source/drain and the substrate leads to store the heat inside the heat zone in SOI transistor.

Two-dimensional temperature distribution contours in the nano-transistors at different times are shown in Fig III.7(a-f). These figures show that the heat diffusion increases in the left and the right of the zone active. It is evident in Fig.7(e) and Fig.7(f) that the temperatures are trapped in the source-drain since the buried-oxide layer acts as a heat cage which hinders the heat from passing into the substrate and causes a remarkable temperature increase inside the SOI transistor. This phenomenon affects the electrical transport in the nano-device, while Fig.7(b) and Fig.7(c) show that most of the heat leaves the MOS transistor to the bottom of the device, where the temperature at the bottom of transistor is 300 K since the heat diffusion in the space is smaller than the mean free path of the material at short time. At 5 ps, Fig.7(a) and Fig.7(d) show that the temperature distribution is the same for both devices because the heat propagation does not reach the oxide layer, hereinafter, the difference is obvious.



(a)



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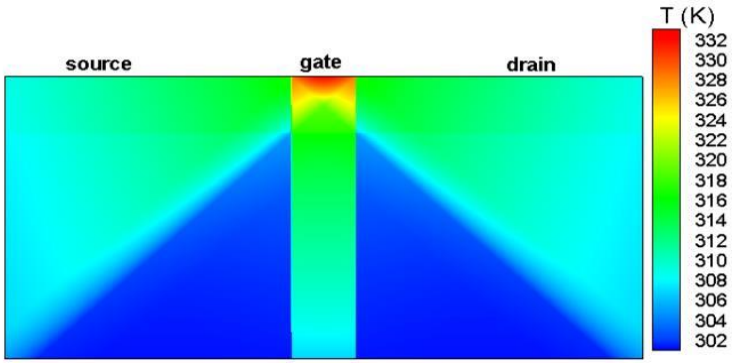
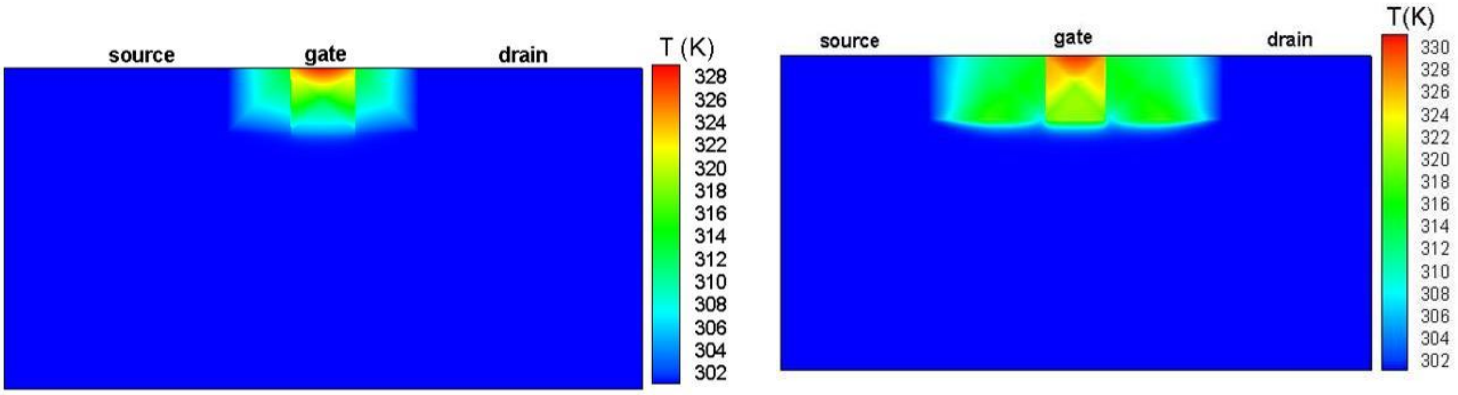
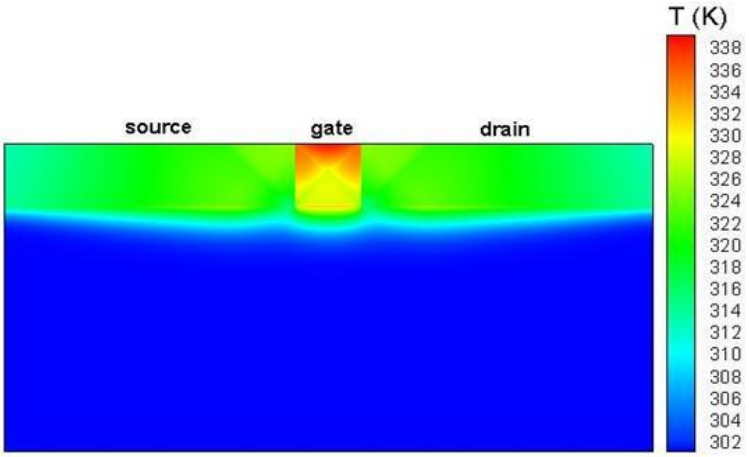


(c)



(d) (e)



(f)

Fig III.7. 2D temperature distribution in the transistors at different times for *Kn*=10:

a) MOSFET at *t*=5 ps, b) MOSFET at *t*=10 ps, c) MOSFET at *t*=30 ps,

d) SOI-MOSFET at *t*=5 ps, e) SOI-MOSFET at *t*=10 ps, f) SOI-MOSFET at *t*=30 ps.

Fig III.8 exhibits the variation of heat flux along the centerline ($x=L/2$) of the nano-SOI MOSFET and conventional MOSFET at different times. The maximum values of heat flux are observed at oxide-semiconductor interface for both transistors, which reach 21.5×10^{11} and 18.7×10^{11} W/m^2 for SOI and MOSFET devices at *t*=30 ps, respectively. At *t*=10 ps, the maximal heat

flux almost converged in the two devices because the influence of the insulation layer has not yet reached the interface. Furthermore, similar to the behavior of temperature, a diminution then augmentation of the heat flux in the channel region and a sharp decline in the heat flux at y =10 nm are noticed due to the heat cage in SOI-MOSFET.

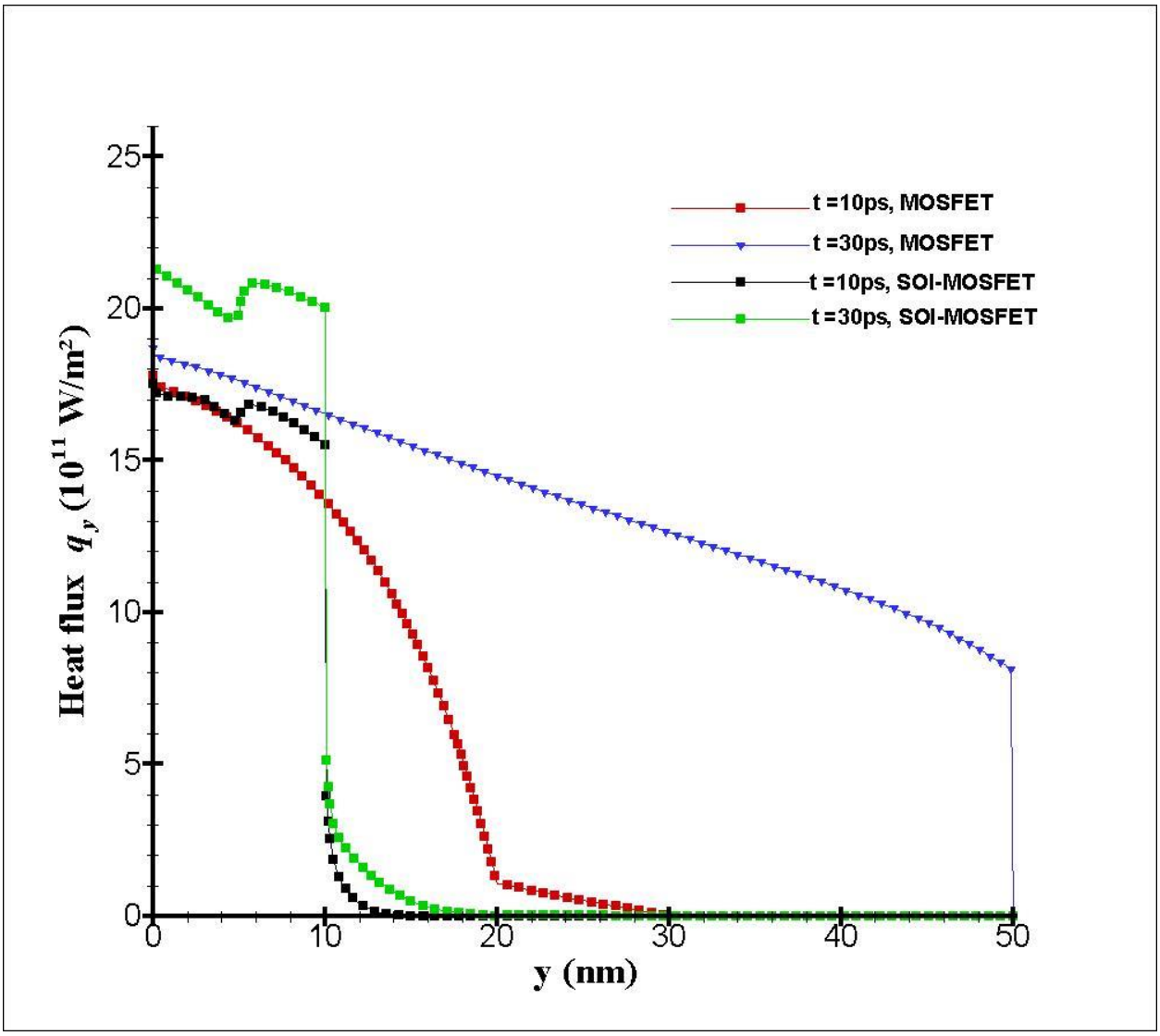


Fig III.8. Comparison of heat flux profiles of the MOSFET and SOI-MOSFET at $x=L/2$ for various times

Fig III.9 displays the temperature versus the x-direction at the centerline of MOSFET and SOI-transistor nano-devices at *t*=30 ps and 10 ps. For both transistors, the form of curves is symmetrical at *x*=50 nm where the maximal temperatures are located. It is obvious that the hot temperature is located in the channel region where the generated heat is transferred to the right

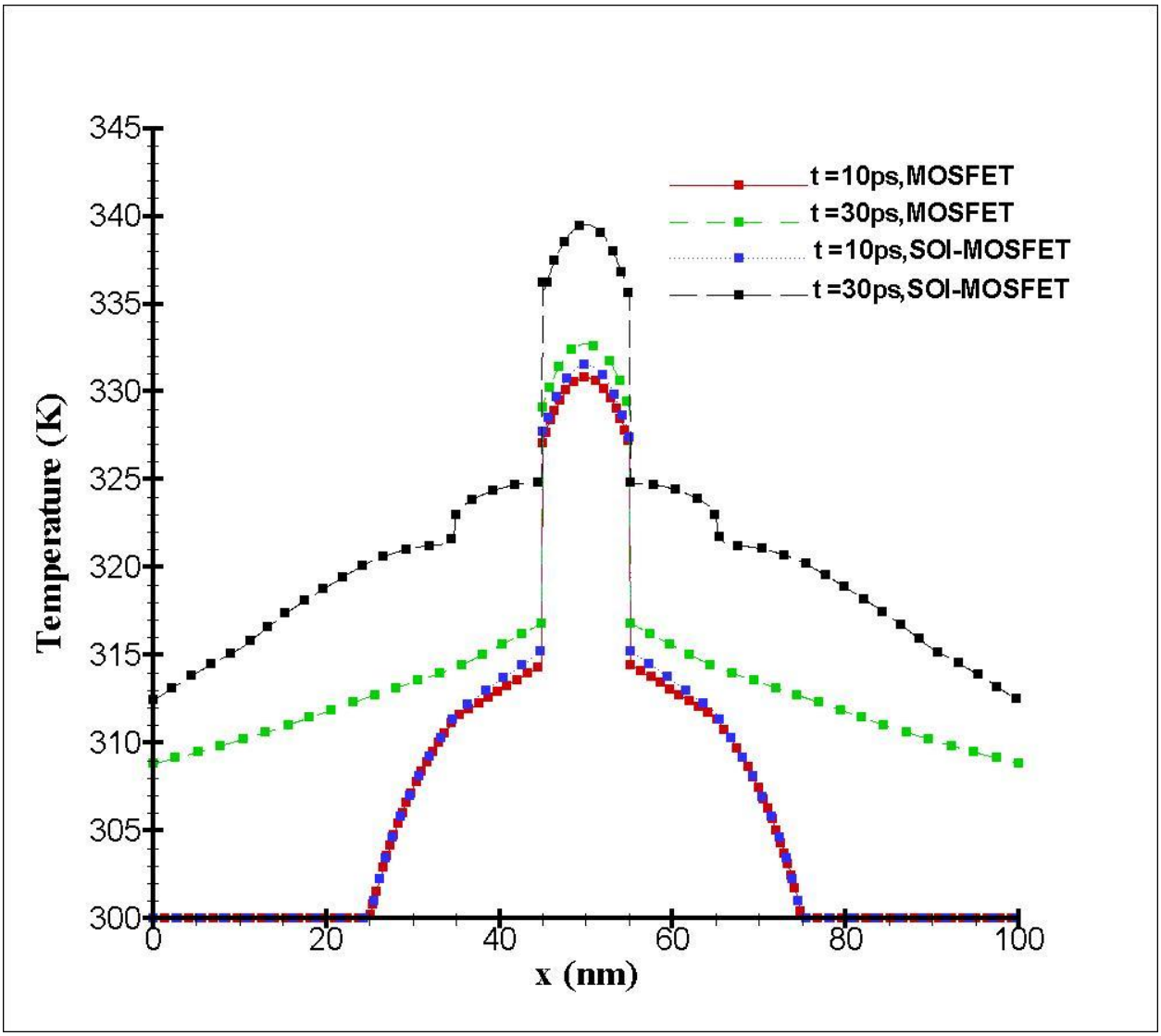


Fig III.9. Temperature distribution at $y = 0$ in the conventional MOS device and SOI MOSFET at $t = 10$ ps and $t = 30$ ps

side and the left side of the active zone. At *t*=10 ps, the temperatures are close for both studied systems, while the temperatures are obviously different at *t*=30 ps due to the effect of the

reduction of thermal conductivity in SiO_2 layer in which it works to increase the heat in SOI transistor.

III.5 Length channel impact

In the previous section, the results of heat transfer inside transistors for *Kn*=10 is discussed. In the rest of this section, the heat conduction within traditional MOS transistor and SOI transistor for *Kn*=5 is evaluated. 2D temperature contours in traditional MOS device and SOI transistor at *t*=10 ps and *Kn*=5 are displayed in Fig III.10. The figure reveals that the increment in the length

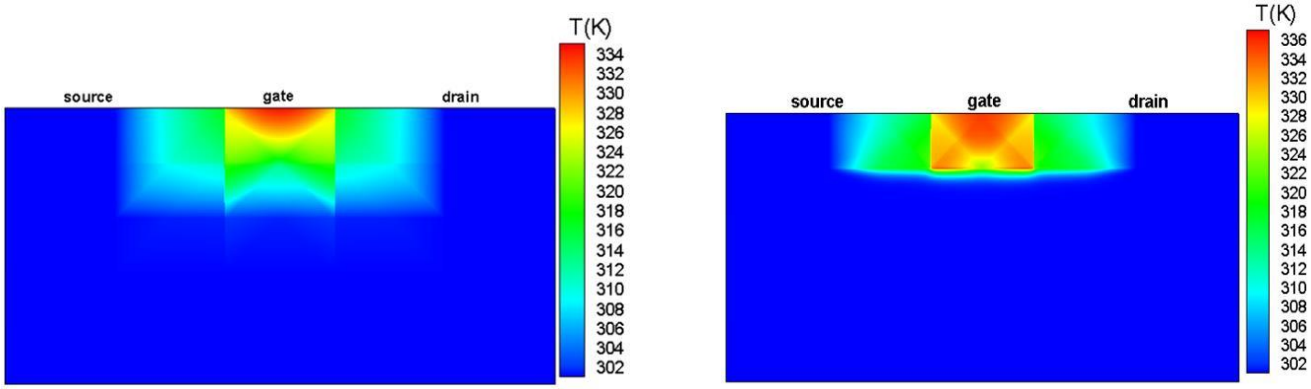


Fig III.10. 2-D temperature distribution in the nano-devices at *t*=10 ps and *Kn*=5: a) MOSFET, b) SOI-MOSFET

of the channel led to a rise in the temperature in the active zone of nano-devices where the maximal hotspot at the interface is 335 K in MOS transistor and 336 K in SOI transistor. This increase of temperature is due to an increase in the area of generated heat and collisions of wall-phonons at interface (Si-SiO_2) while the low thermal conductivity of oxide results in the temperature increase in the SOI device. The heat diffusion dissipates in the left and right sides of the heat zone for both devices and it is conducted toward the bottom of MOS device.

Fig III.11 presents the temperature difference ($T-T_{ref}$) variation versus the vertical centerline of the nano-MOS transistor and SOI-MOSFET for *Kn*=5. From the curves of the present model, it is

seen that the temperature is increased with the increase of time in both transistors. At *t*=10 ps, the maximal peak temperatures are spotted at the interface then it decreases until it stabilizes in the substrate. However, at *y*=10 nm, there is an influence of decrease in the thermal conductivity of

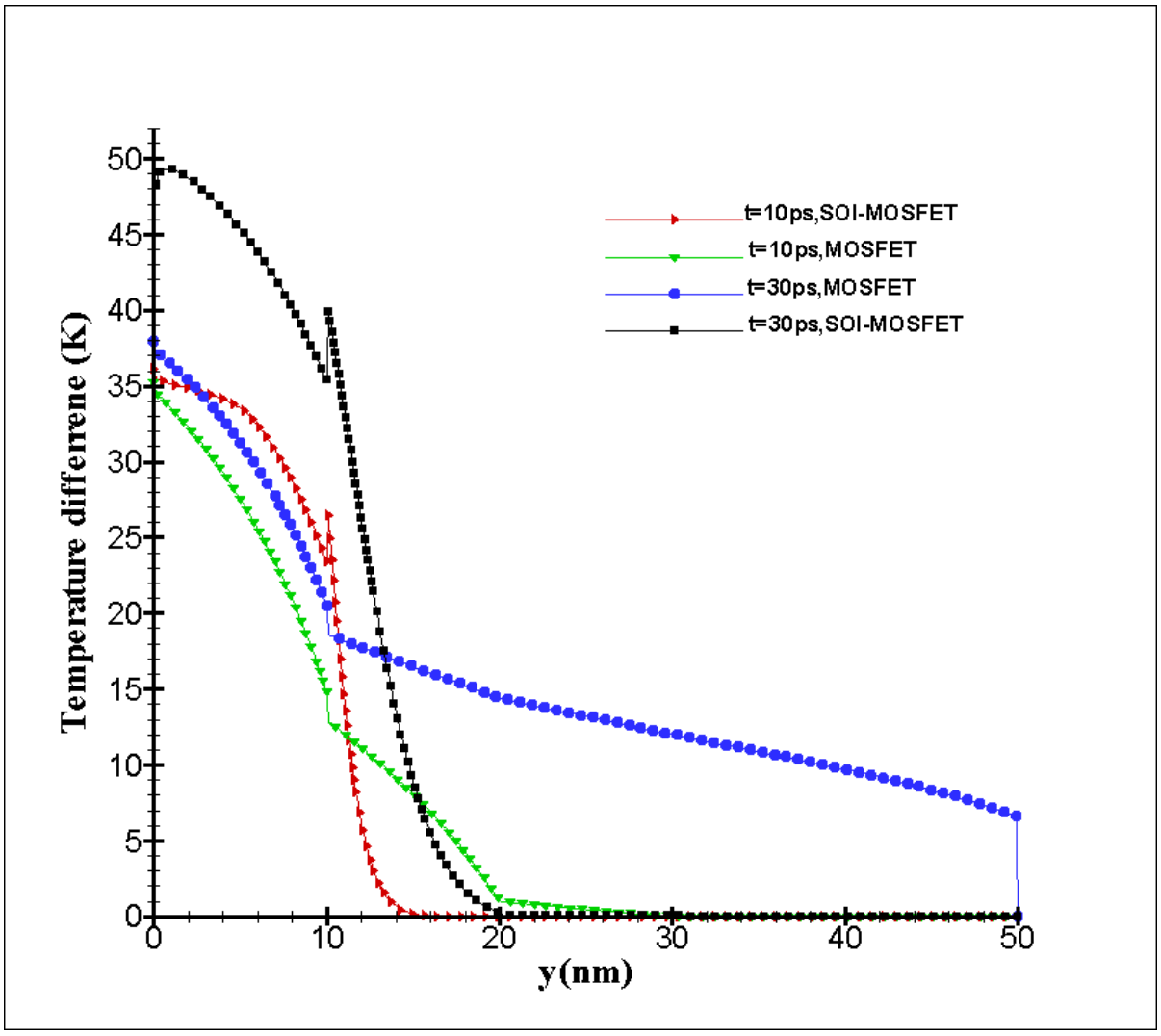


Fig III.11. Temperature profiles along y-direction in the centerline of the MOSFET and SOI-MOSFET at various times (*Kn*=5)

the oxide silicon which led to a strong temperature increase. At t = 30 ps, it is seen that the maximal hotspots are 38 K and 49 K for MOSFET and SOI device, respectively. This thermal growing is because of collisions of electrons-phonons (Joule effect) and the increase on the surface collisions of wall-phonons at interface with the effect of the dielectric layer at the SOI device.

Fig III.12 shows the evolution of heat flux along the vertical centerline of the nano- transistors for Kn=5. It is seen that the maximum heat flow is noticed at the oxide-semiconductor in MOS transistor interface, while it is located in the heat zone for SOI-MOSFET where the maximal heat flux reaches 19.3×10^{11} W/m^2 and 26.4 $\times10^{11}$ W/m^2 at t=30 ps for MOS and SOI transistors, respectively. At t=30 ps, in the bottom boundary of MOSFET, the heat flux is decreased due to the regime ballistic from a transport carrier (Kn >1) and the length of the channel region is less than the mean free path of silicon. The oxide layer in SOI transistor with augmenting the length of channel region (20 nm) leads to store heat within the active channel, which causes elevation of the thermal generation with time. This in turn leads to an increase in the temperature and heat flux inside the channel region compared to the semiconductor–oxide interface at t = 30 ps.

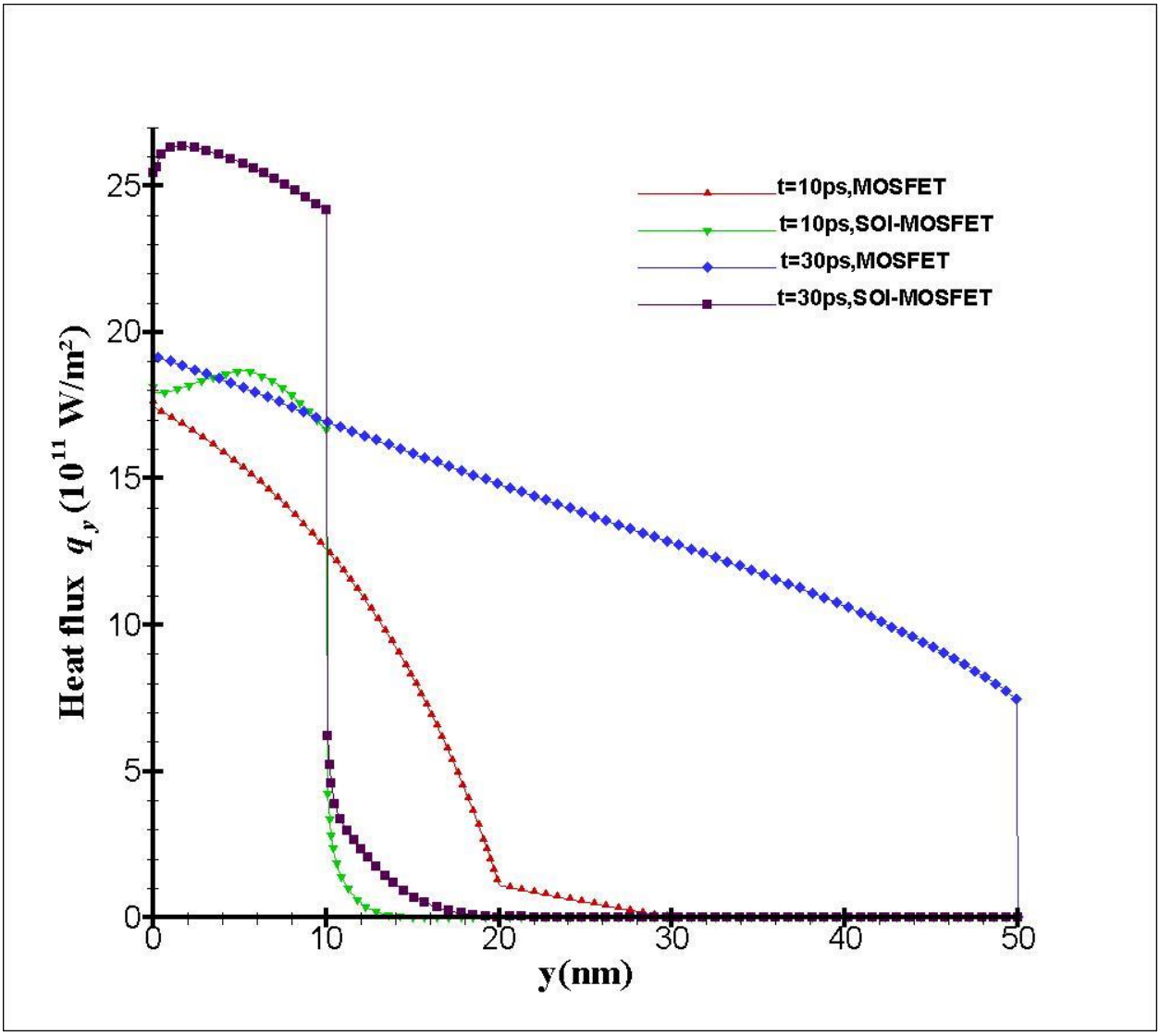


Fig III.12. Comparison of heat flux profiles of the MOSFET and SOI-MOSFET at $x=L/2$ for various times (Kn=5)

III.6 Robin condition influence

The aim of the present study is to examine the influence of Robin boundary condition on the heat transfer of nano-devices. Since information about manufacturing nano- transistors devices in terms of dimensions and materials is not public due to competition between manufacturers, this information is blocked. Thus, the necessary data have been obtained from the previous works in the literature [4, 8, 9, 16, 53, 68]. The right side and left side boundaries in the nano-MOSFET and the SOI-MOSFET are assumed adiabatic. On the other hand, the bottom boundary is

supposed to be isothermal (300 K) and the top boundary (source/drain) is subjected to Robin boundary condition, where the conduction process and the convection process are in equilibrium. This boundary condition is defined as [16, 35, 85]:

$$-k\frac{\partial T}{\partial y}=\frac{(T-T_0)}{R_{th}} \tag{III.7}$$

where R_{th} stands for the thermal contact resistance and T_0 is the ambient temperature.

The dimensionless Robin condition is represented as follows:

$$-\Lambda^{*}\frac{\partial T^{*}}{\partial y^{*}}=\frac{3T^{*}}{CvR_{th}}=\frac{1}{R_{th}^{*}}T^{*} \tag{III.8}$$

Robin boundary condition is applied at the top boundary where the drain and the source are located.

$$u_i^{*}(x^{*},0)=\frac{u_i^{*}(x^{*},1)}{1+(\Delta y^{*}\times\frac{1}{\Lambda^{*}\times R_{th}^{*}})} \qquad i=1..8 \tag{III.9}$$

In the present work, a study on the sub-continuum 2D heat transfer within nano- MOSFET and SOI-MOSFET is reported employing the LBM D_2Q_8 model coupled with Robin condition and temperature jump condition type at Kn = 10. In addition, the thermal resistance varies between $R_{th}=10^{-7}$ and 10^{-10} m²·K/W [16, 35].

III.6.1 MOSFET case

Fig III.13 compares the temporal peak temperature (T-T_{ref}) at x=L/2, y=0 of the nano-MOSFET with different thermal resistances at Kn =10. The results of the present LBM model are compared with those of other models. For the case of without thermal resistance (R_{th}^{-1}=0), the curve of peak temperature is reached a steady-state (saturation) at 15 ps. This result is confirmed by the SPL [9] model simulation. But, it is evidently seen that the temperature escalates sharply in the DPL model [46] due to larger gradient temperature gradients in DPL equation. The peak temperatures are 32.4 K, 24.8 K and 19.7 K respectively for the present, DPL and SPL models.

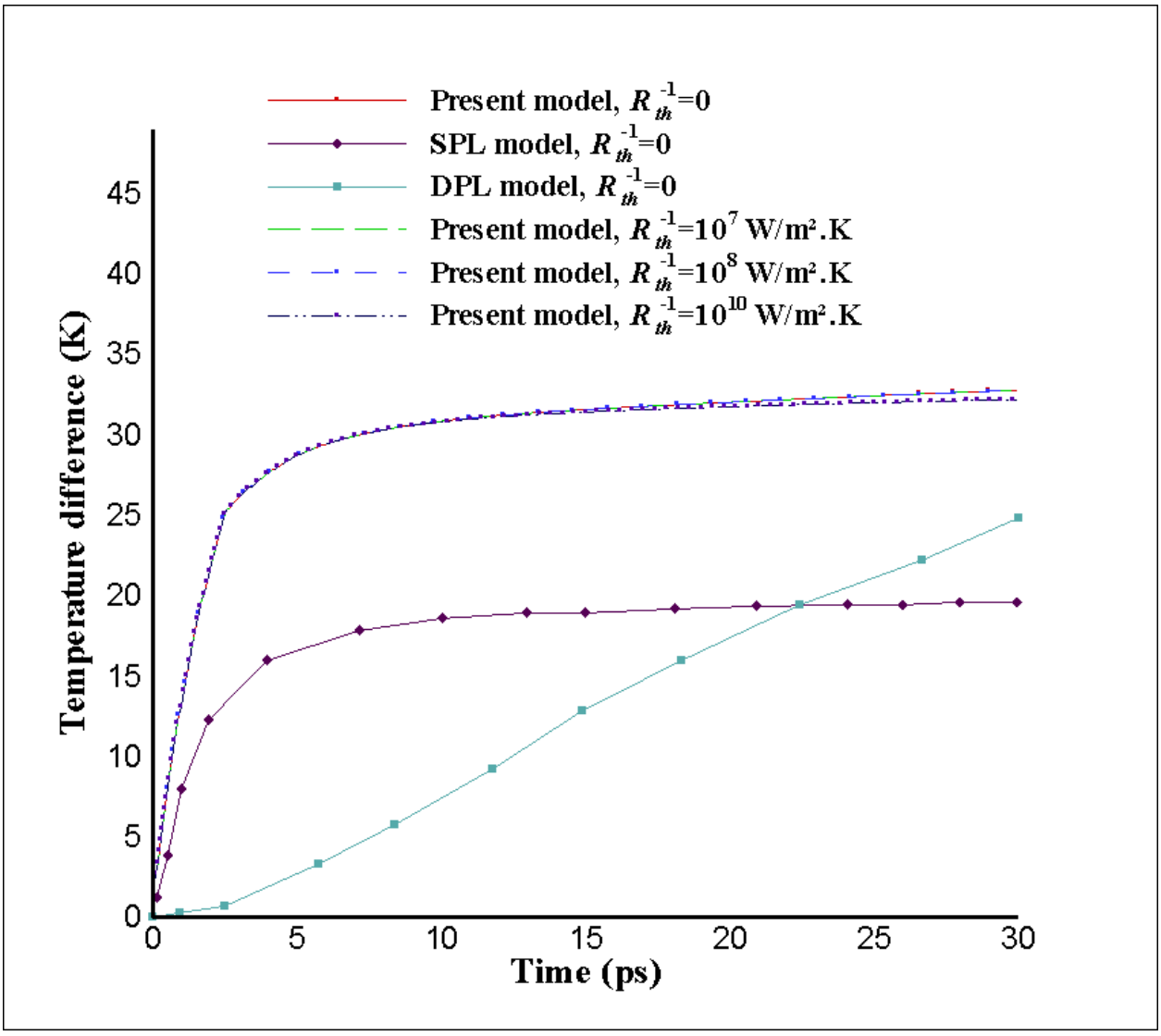
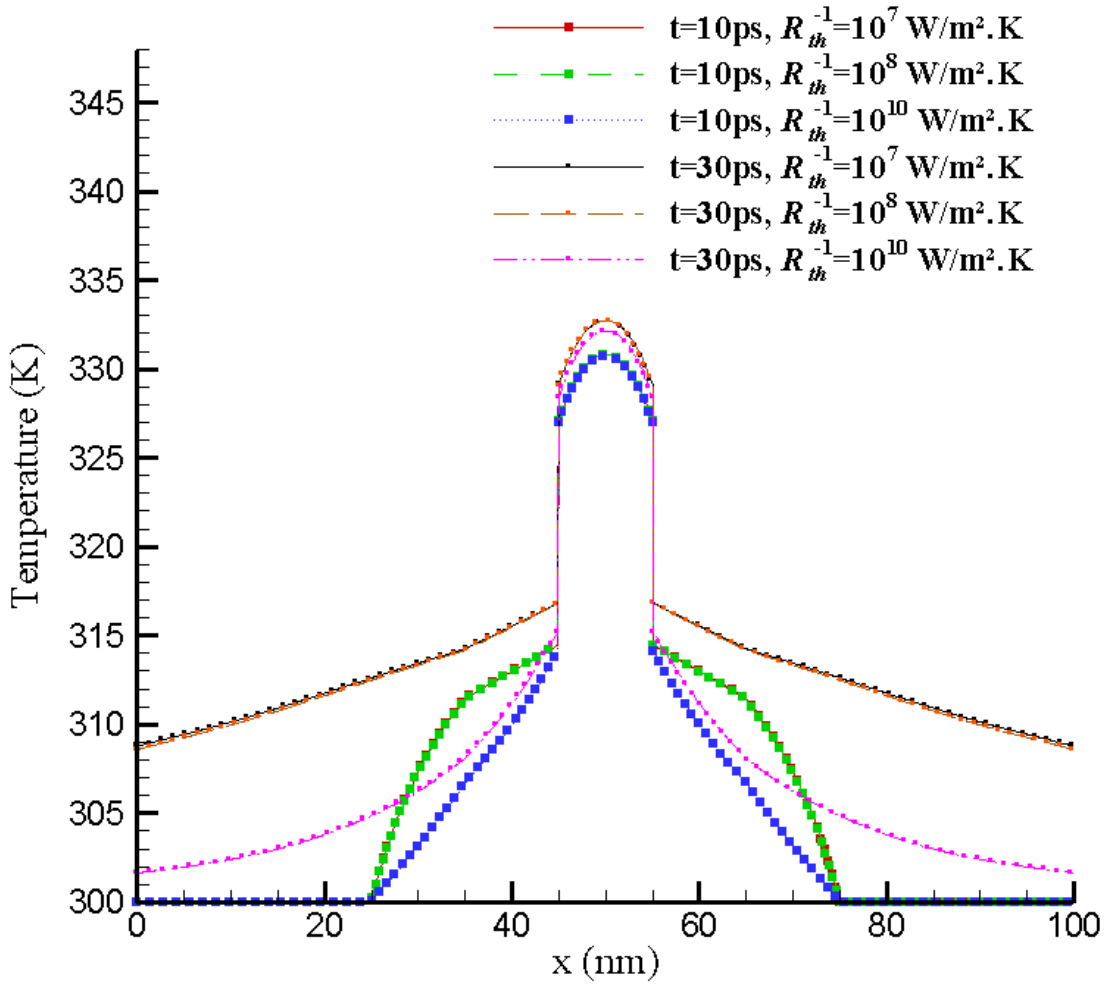


Fig III.13: Comparison of the temperature difference in the centerline of the MOSFET

Furthermore, it is obvious that in the peak temperatures in the present suggested model are nearly the same for both thermal resistances of $R_{th}^{-1}=10^7$, 10^8 and 10^9 W/m^2·K, while there is a slight decrease for 10^{10} W/m^2·K, where it reaches 31.7 K and the temperature starts decreasing at 20 ps. The results of our present model show that the jump condition at the interface with Joule effect is dominated by the convective condition at the source/drain.

Fig III.14 shows the temperature profiles along *x*-direction at *y* = 0 for different times and thermal resistance values. It is evident from the results that the temperature increases with elapsing time and there are high temperatures at the active channel due to the phonon-wall



FigIII.14: Temperature profiles along *x*-direction at *y* = 0 in the MOSFET for different times and thermal resistances.

collision and electron-phonon collision. In addition, the thermal resistance R_{th}^{-1} =10^{10} W/m²·K show an effective behavior in eliminating heat compared with R_{th}^{-1} =10^{7} and 10^{8} W/m²·K. On the other hand, it is noticed that there is no effect in the channel region where the effect of heat generated is greater than convective process. At 30 ps, the temperature reaches 309 K for R_{th}^{-1}=10^{7} and 10^{8} W/m²·K, and 302 K for R_{th}^{-1} =10^{10} W/m²·K at *x*= 0 and 100 nm, respectively.

Fig III.15 presents temperature variation versus *y*-direction at the centerline ($x=L/2$) for different thermal resistances at 10 ps. The maximal temperature is noticed at interface semiconductor-oxide in our LBM model and DPL model [46]. The difference in the maximal values and curves

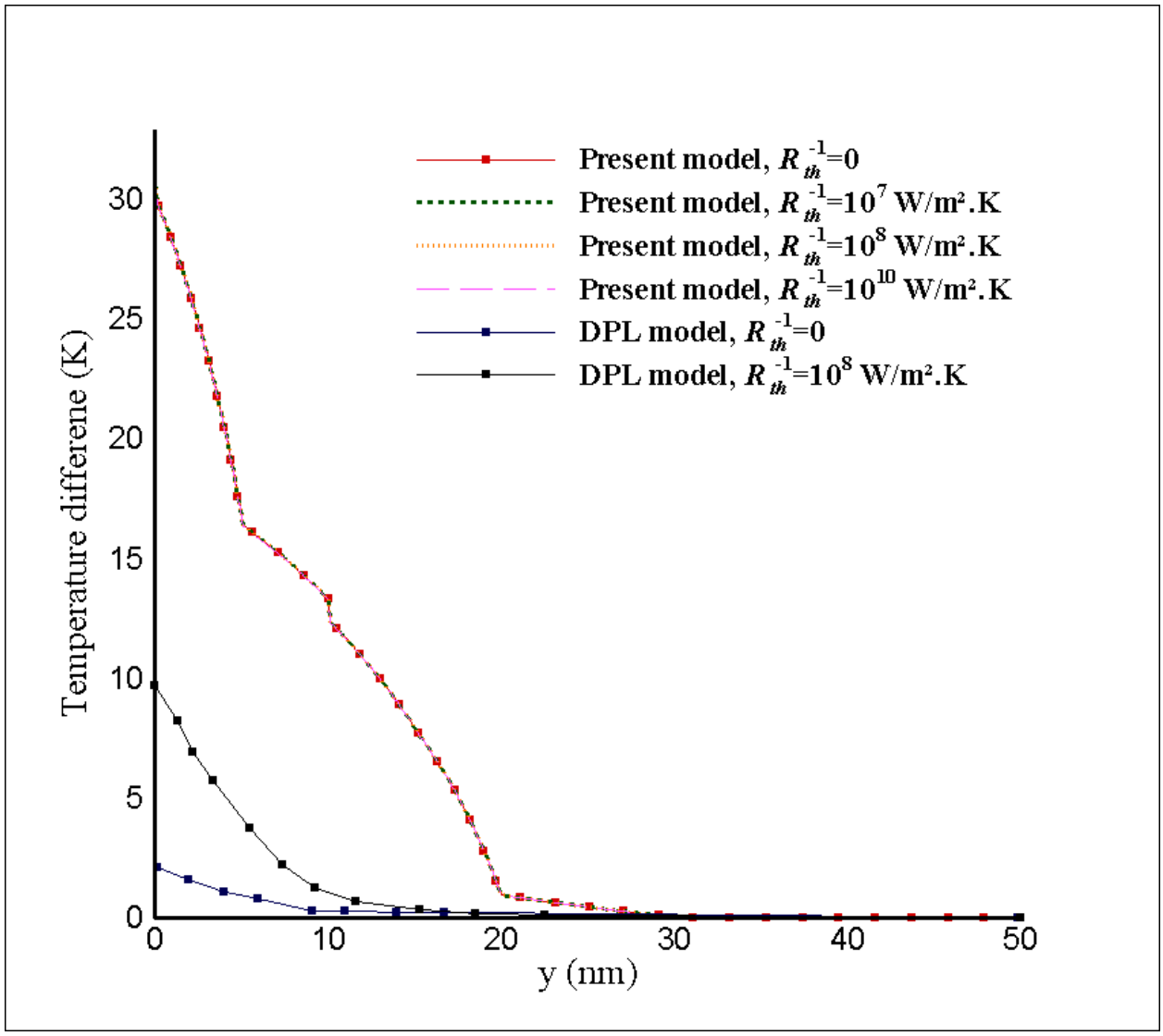


Fig III .15: Comparison of temperature difference in *y*-direction at the centerline ($x=L/2$) of the MOSFET for different thermal resistances at t = 10 ps.

is due to the methodology used to study the collision at Si/SiO_2 and the heat transfer by the phonons where the present model employs a mesoscopic method, while the DPL model utilizes a macroscopic method. Furthermore, the DPL model includes an additional term whereas the present model does not have this term, which is a preference for the LBM model. Moreover, it is clearly seen that the temperature profiles are the same for different thermal resistances $R_{th}^{-1}=10^{7}$,

10^8, 10^9, and 10^{10} W/m²·K in the proposed model since the convective term has no effect at this time (t = 10 ps) yet.

2D effects of the thermal resistance on temperature distribution at t=30 ps are presented in Fig III.16. It is obvious that the temperature keeps a symmetry to centerline (x=L/2) of the MOS transistor for these three figures and the temperatures are maximal at the interface of Si-SiO_2. For

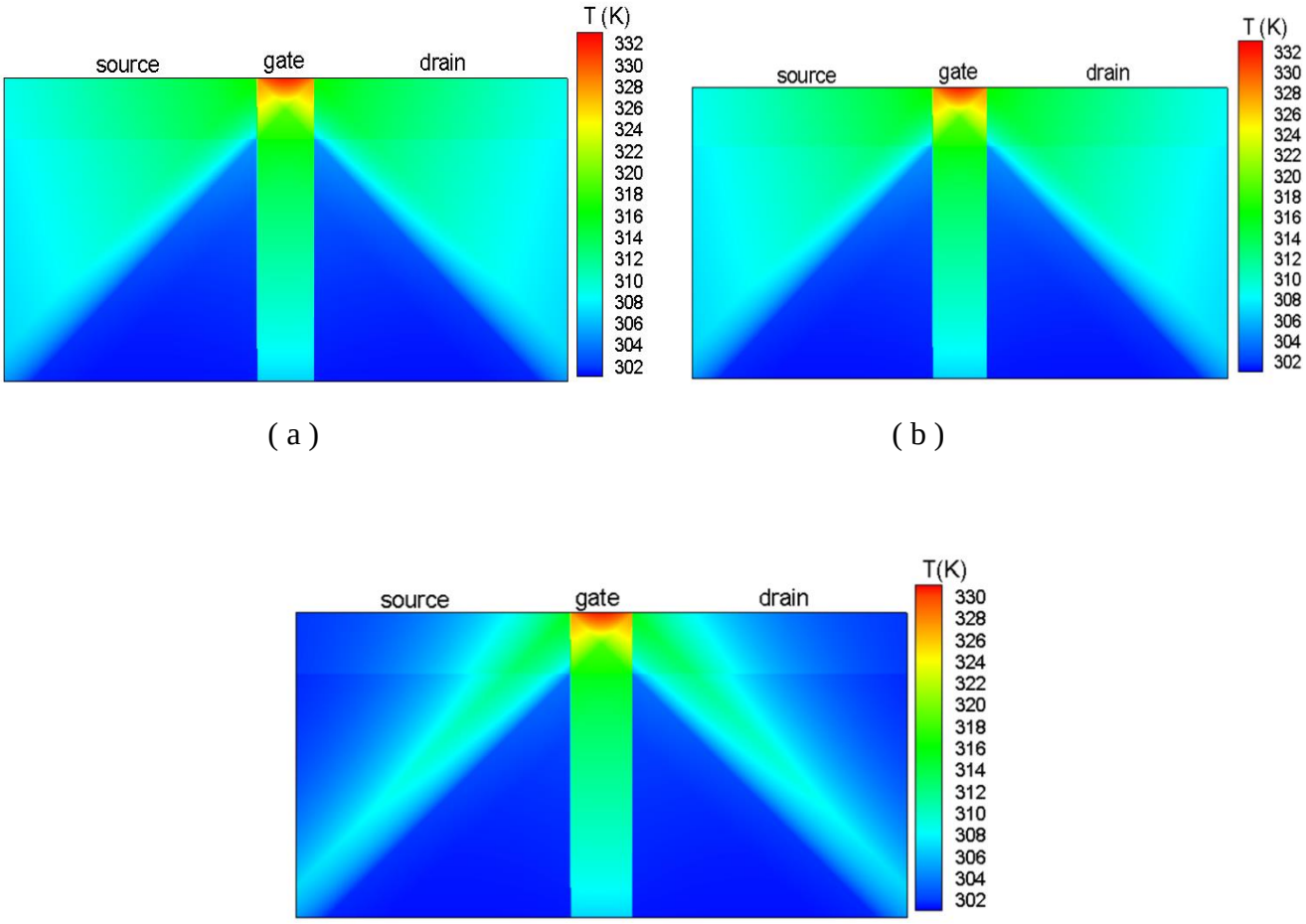


Fig III.16: 2D temperature distribution in MOSFET at t = 30 ps a)R_{th}^{-1}=10^7 W/m²·K, b) R_{th}^{-1}=10^8 W/m²·K , c) R_{th}^{-1}=10^{10} W/m²·K

R_{th}^{-1}=10^7 W/m²·K and 10^8 W/m²·K, temperature maps are nearly the same where the maximal temperature reaches 332.4 K for both thermal resistances. So, the convective terms have no role in decreasing the hotspot in the active zone (channel region) and bulk silicon structure. On the other hand, from the temperature distribution for R_{th}^{-1}=10^{10} W/m²·K, shown in Fig.16(c), it is

seen that the temperature in the bulk of device at the source/drain is lower compared with the other thermal resistances while the maximal temperature at the interface is estimated 331.7 K. Hence, the convective term plays a role in declining the temperature in the right and left sides of the channel region. The form of temperature distribution in these three figures reveal that the intensive heat diffusion has occurred in the bottom substrate where the low temperature is located since the space of phonon transport is less than the mean free path of the semiconductor .

FigIII.17 displays the evolution of heat flux versus y-axis in centerline of MOS nano-transistor at

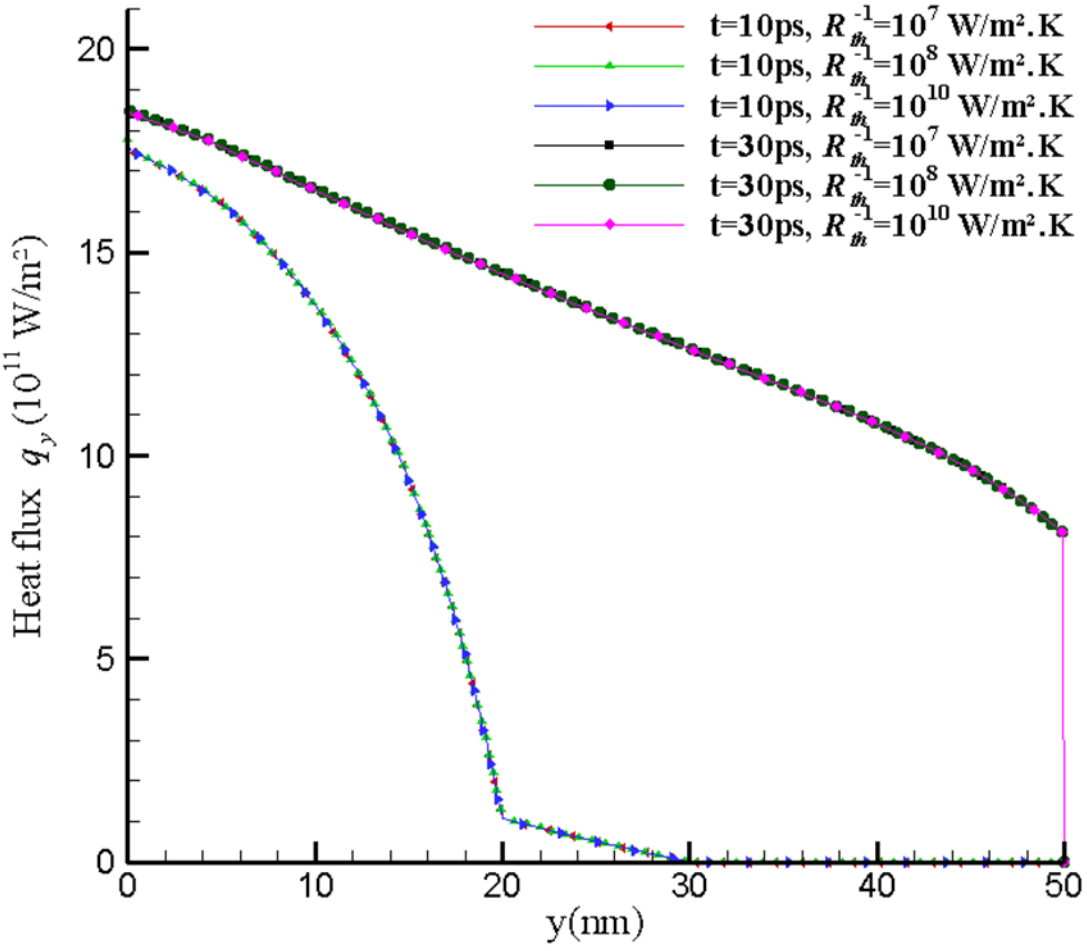


Fig III. 17: Heat flux profiles in *y*-direction at the centerline (*x*=*L*/2) of the MOSFET for different thermal resistances.

time scales of *t* =10 ps and 30 ps with different thermal resistances. It is clear that the maximal heat flux is located at the interface due to phonon-wall collision at the interface. Furthermore, the

heat flux increases with time and reaches 17.7×10^{11} W/m² at t =10 ps and 18.7×10^{11} W/m² at t =30 ps. Moreover, the thermal resistance has shown no influence on the heat flux along the centerline of nano-transistor due to the dominant of the jump condition effect at the interface.

III.6.2 SOI-MOSFET case

The device called SOI-MOSFET is similar to the conventional MOSFET, however, it includes an additional layer of insulator (SiO2) in order to reduce the current leakage to substrate from the drain/source junction. Moreover, it is worth noting that a smaller coupling capacitance from the conducting channel is introduced by this insulation layer.

Comparison between the present proposed model and CV model for different thermal resistances in SOI-transistor at $x = L/2$, $y = 0$ is presented in FigIII.18. The analysis of variation of thermal behavior with time exhibits that the temperature obtained by the CV model [16] is not saturated irrespective of excluding or including thermal resistance. On the contrary, the temperature saturates at 15 ps with the present model. These interesting results could be explained by the fact that the phonon energy density is in the status stability at the interface in the present LBM model. But the diffusive part in the CV model is low, which caused thermal instability and an increase in temperature with time. From the curve of CV model, the reduction of the peak temperature reaches 51.8 K for $R_{th}^{-1}=10^{10}$ W/m²·K at 30 ps whereas it reaches 80 K without the thermal resistance ($R_{th}^{-1}=0$). In the present model, the temperature profiles for $R_{th}^{-1}= 0$, 10^7, 10^8 and 10^9 W/m^2·K overlap and the temperature reaches 39.6 K, while further increase in the thermal resistance $R_{th}^{-1}=10^{10}$ W/m²·K reduces the saturation temperature to 38.5 K.

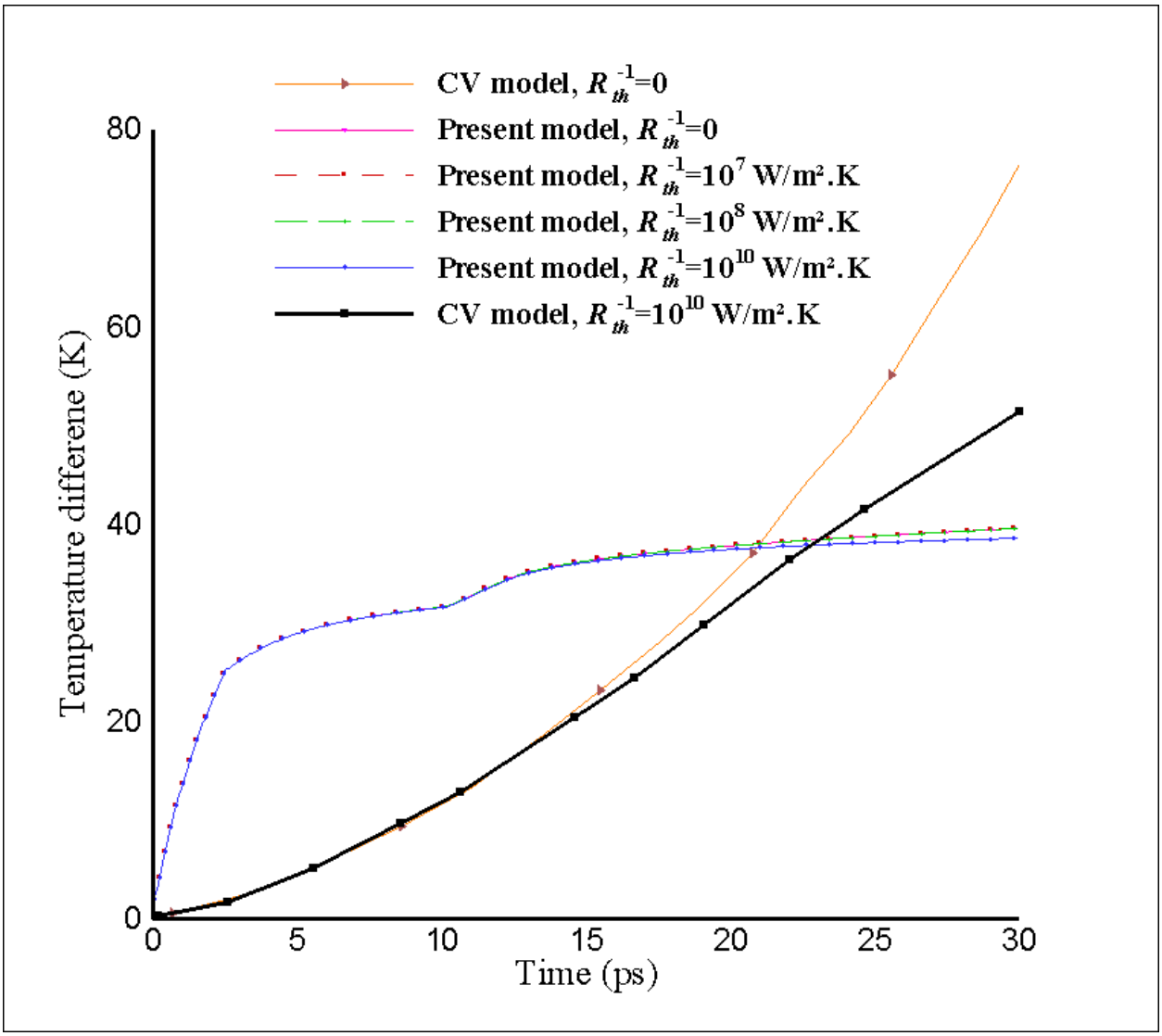


Fig III.18: temperature difference at $x=L/2$, y = 0 of the SOI- MOSFET for different thermal resistances.

Fig III.19 shows the temperature profiles at centerline ($x=L/2$) along y-direction in the SOI device at 30 ps for different thermal resistances. In general, it seems that the temperature is maximal at the interface of Si-SiO_2 (y = 0) due to the phonon–wall collision. A comparison of the two models at $R_{th}^{-1}=10^{10}$ W/m²·K reveals the smoothly varying temperature gradient in the channel region. Hereinafter, the temperature declines in the CV model at the substrate because of the low thermal conductivity in the layer oxide. Meanwhile, it can be noticed that the temperature rises at y=10 nm in the present model since the thermal resistance in the SiO_2 layer

obstructed heat diffusion to the substrate, which led to heat storage inside the channel. The temperature profiles for $R_{th}^{-1}=10^7$, 10^8, and 10^9 W/m^2·K are the same.

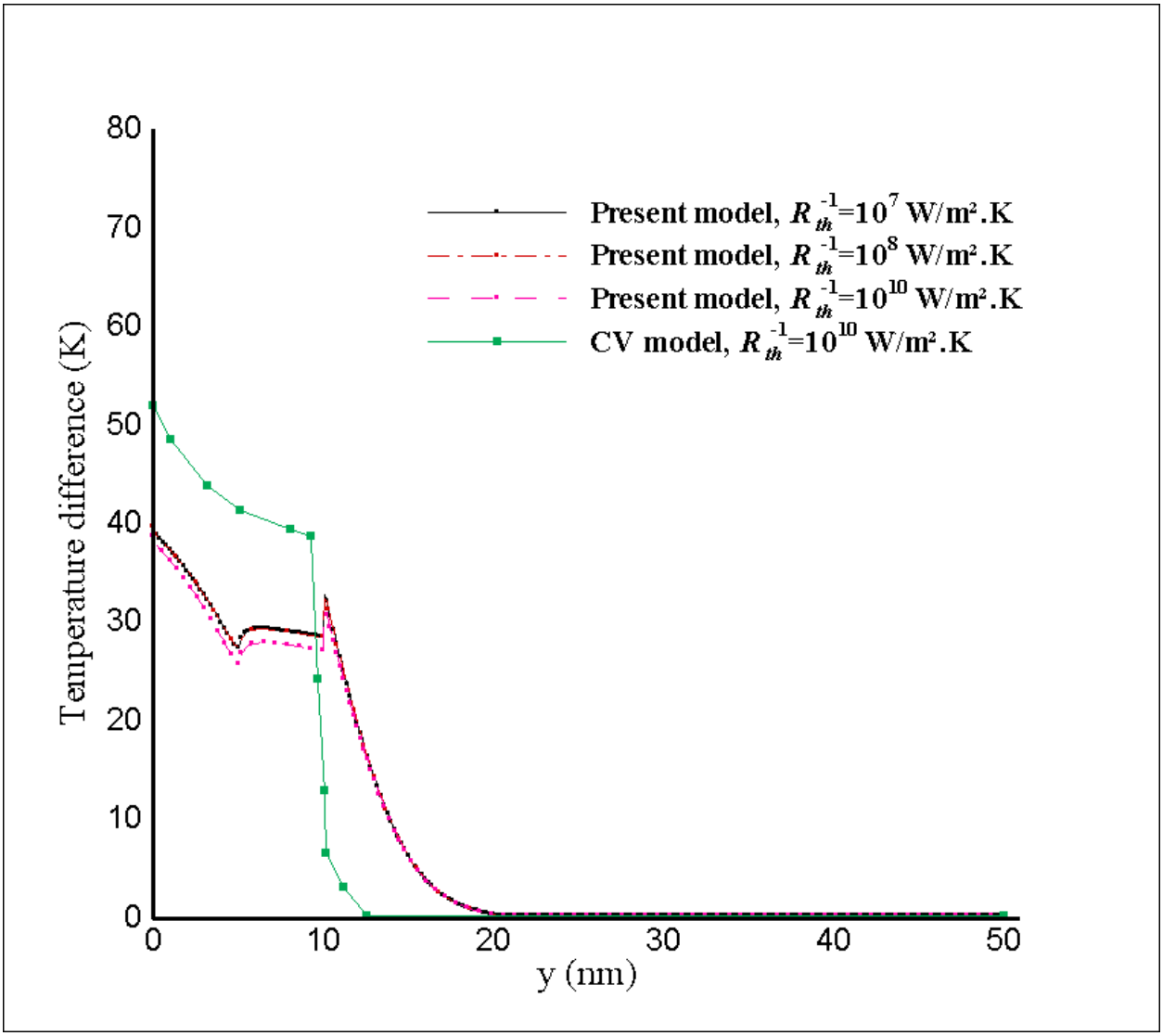


Fig III.19: temperature difference in *y*-direction at the centerline of the SOI-MOSFET for different thermal resistances at t = 30 ps.

Fig III.20 shows the temperature profiles along x-direction at y = 0 in SOI-MOSFET for different times and thermal resistances. It is clear that the curves are symmetric in x=50 nm for various times and thermal resistances while the temperatures are increased with time increases. At t =10 ps, the temperature does not change in the channel region at three different thermal resistance values but the temperature decreases in left side and right side of the channel region for $R_{th}^{-1}=10^{10}$ W/m²·K. On the other hand, at t = 30 ps, the maximal hotspot is reduced for R_{th}^{-1}=

10^{10} W/m²·K with a remarkable reduction of temperature in the left side and right side because the heat is extracted out to the external medium by the convection process (Robin condition).

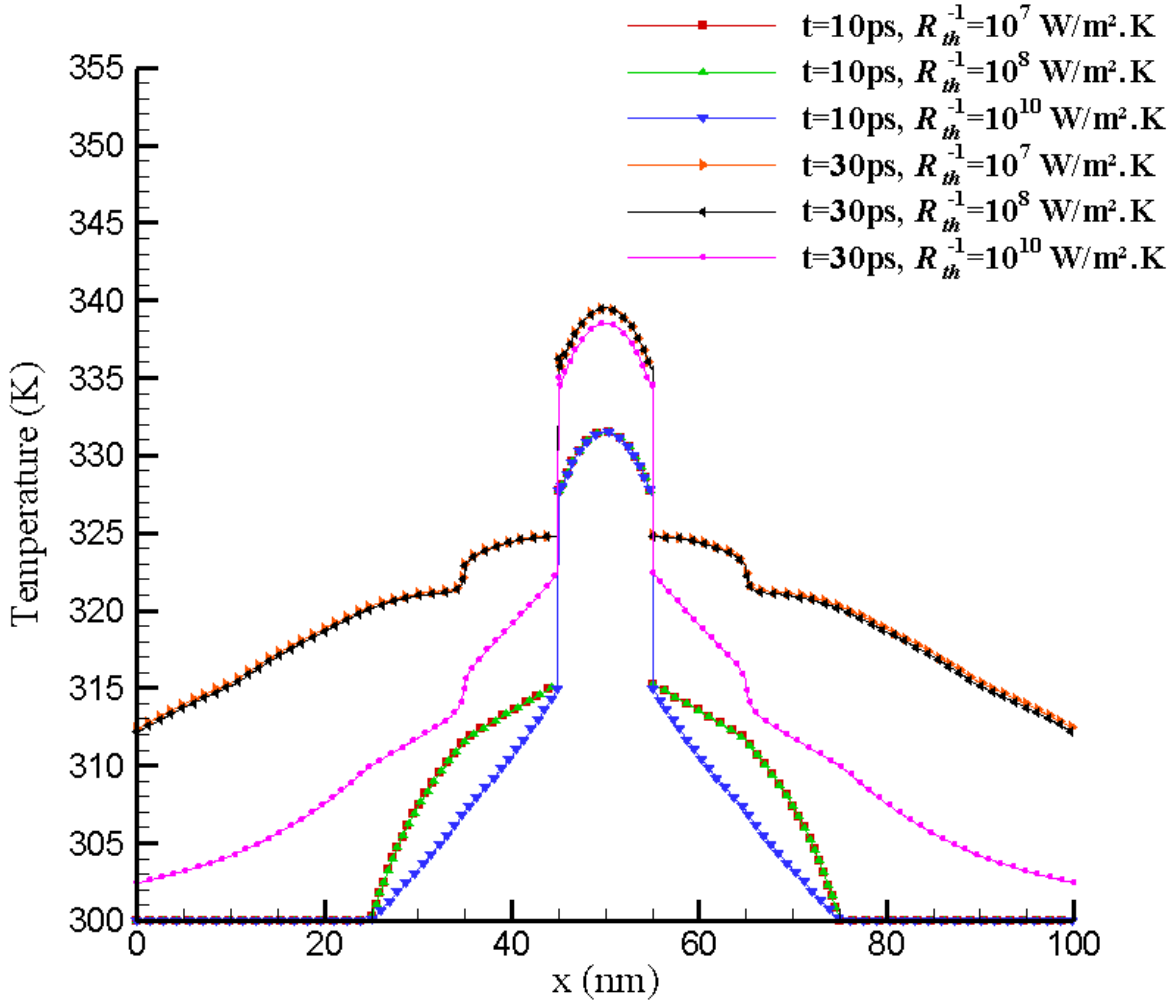


Fig III.20: Temperature profiles along *x*-direction at *y* = 0 in the SOI-MOSFET for different times and thermal resistances

Fig III.21 presents the effect of thermal resistances on 2D temperature distribution in the SOI device at *t*=30ps with corresponding Table 2. The values of high heat are located between the source and the drain without passing it to the substrate due to oxide layer and the temperature is the maximal in the active zone where the heat is generated. For the convective resistances of $R_{th}^{-1}=10^7$ and 10^8 W/m²·K, the temperature distribution is nearly the same. However, for $R_{th}^{-1}=10^{10}$ W/m²·K, lower temperature distribution is observed since the heat is removed by the convection

process represented by the Robin condition in the source/drain, which exhibits the functional role of this term to decrease the temperature.

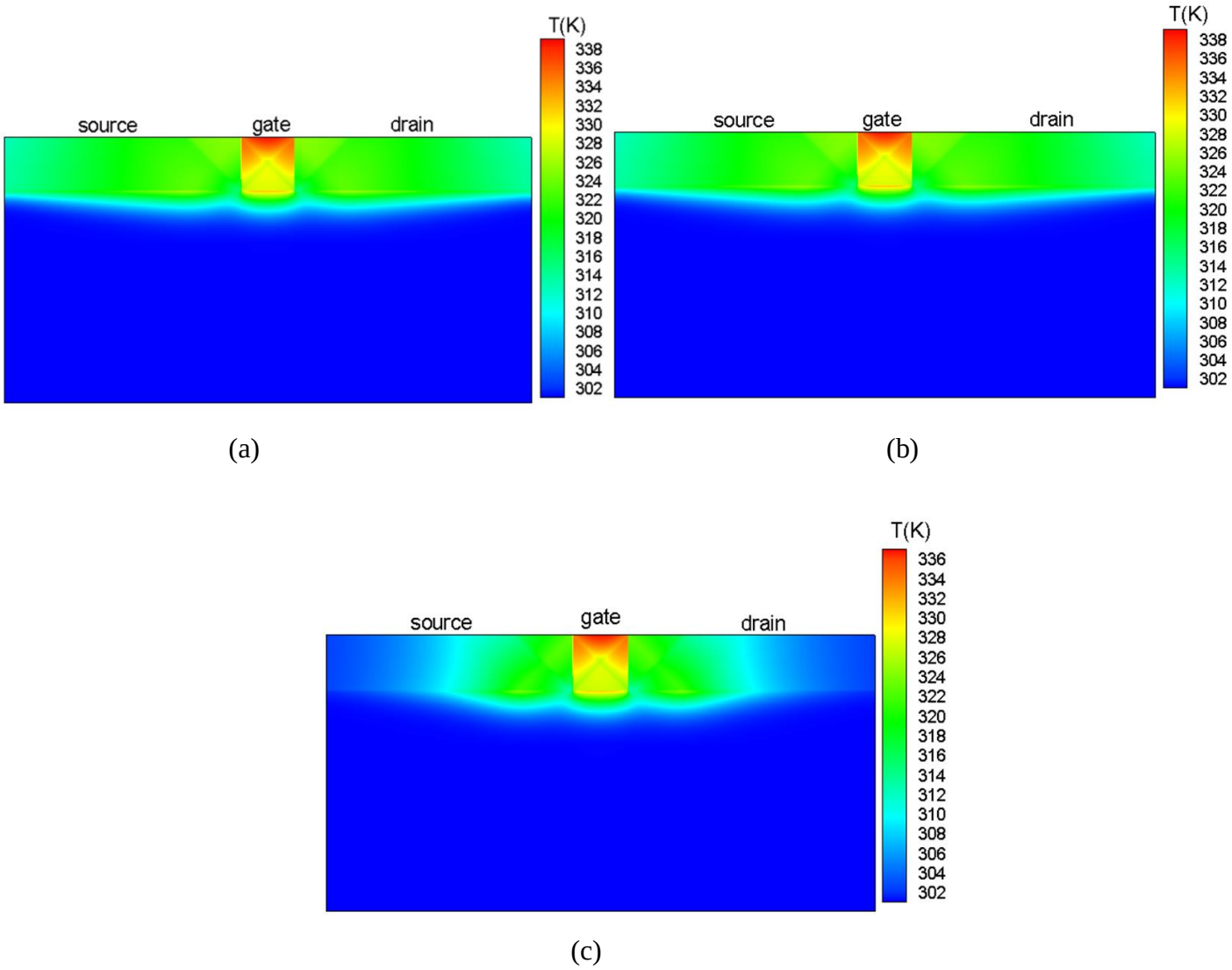


Fig III.21: 2D temperature distribution in SOI-MOSFET at t = 30 ps :

a)$R_{th}^{-1}=10^{7}$ W/m²·K, b) $R_{th}^{-1}=10^{8}$ W/m²·K, c) $R_{th}^{-1}=10^{10}$ W/m²·K

Fig III.22 displays temporal heat flux along y-direction in centerline of SOI transistor at different thermal resistances. As shown in the graph, there is no difference in heat flux profiles for different thermal resistances at t =10 ps whereas the heat flux reduces to 21.2×10^{11} W/m² for $R_{th}^{-1} = 10^{10}$ W/m².K at t =30 ps due to removal of the heat by effect of Robin condition.

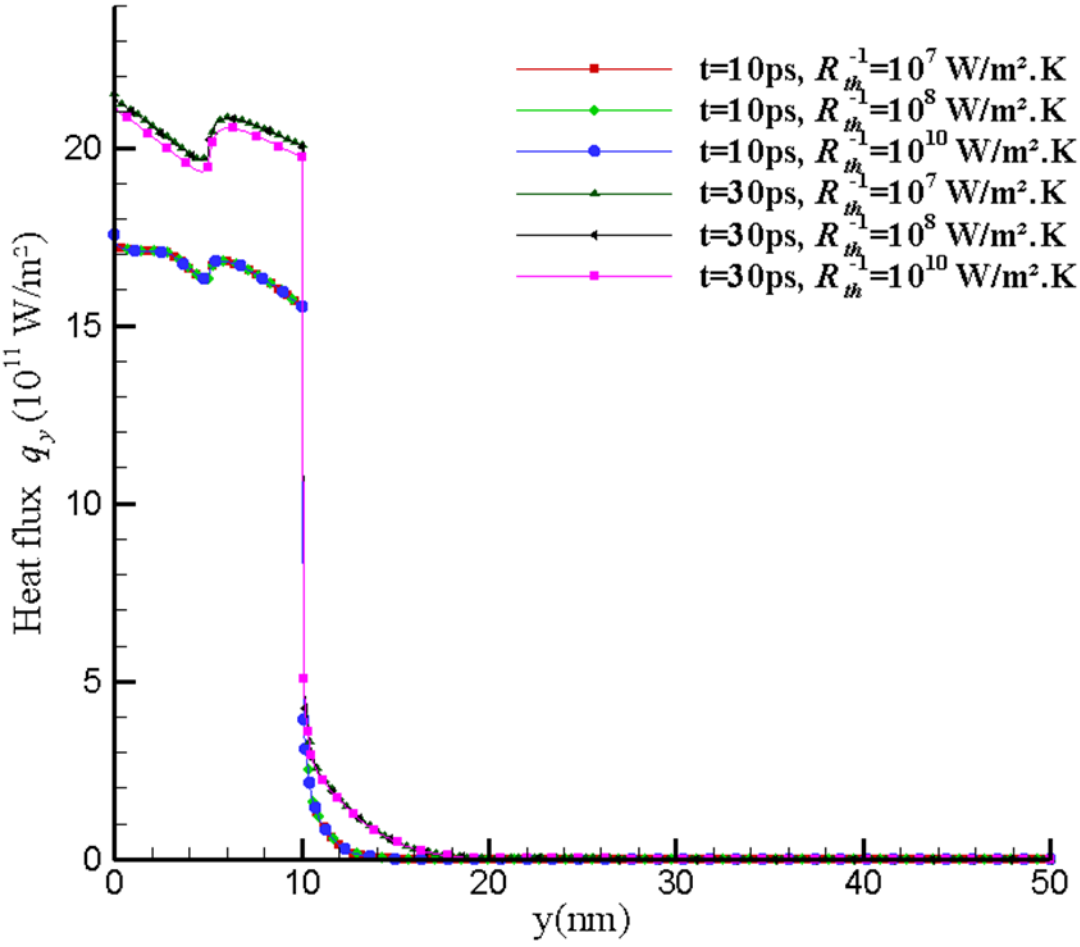


Fig III.22: Heat flux profiles in *y*-direction at the centerline (*x*=*L*/2) of SOI transistor for different thermal resistances.

III.7 Conclusion

The main goal of the current study is to determine the heat transfer in a two-dimensional sub-length of 100 nm conventional MOS transistor and SOI transistor devices considering the LBM D_2Q_8 model integrated with the temperature jump condition type at the presence of a permanent heat source in the heat zone. The results were evaluated for two transistors conformable to actual conditions. The advantage of the model proposed in this study is that it considers the phonon transport with collision phonon-wall in the sub-continuum media compared to the approaches of other models. It is found that the heat flux and temperature are lower in the conventional MOS

transistor compared with SOI-MOSFET where the temperature at *Kn*=10 reaches 339.6 K and 332.4 K at 30 ps for SOI-MOSFET and MOSFET, respectively, while the heat flux reaches 21.5×10^{11} W/m^2 for the SOI device and 18.7 $\times10^{11}$ W/m^2 for the MOS transistor. The insulating layer in the SOI transistor has a negative effect on the thermal distribution, as it attenuates heat release. In addition, increasing the length of channel region causes an increase in the heat inside nano-transistors. At *Kn*=5, the temperature is estimated to be 349 K for SOI transistor, and 338 K for the conventional MOS device. So, this may be considered that nano-transistors are thermally more stable at *Kn*=10, compared to at *Kn*=5. The majority of the heat produced within the MOS device is dissipated to the surroundings and concentrated downwards. Also, we determined the impact of Robin condition with TJBC on the thermal behavior of nanoscale MOSFET and SOI-MOSFET at *Kn* = 10 using the lattice Boltzmann methodology for the operating time up to *t*= 30 ps. This is the first study using LBM D_2Q_8 model to investigate the effect of Robin condition in nano-devices. In general, the simulation results show that in SOI transistor and MOS transistor the maximal hotspot is located at the interface of semiconductor-wall. Also, the results obtained by the present model exhibit that the convective term $R_{th}^{-1}=10^{10}$ W/m²·K is effective to reduce the temperature in the source/drain for both MOSFET and SOI-MOSFET although its influence reduces in the channel region of transistors where the temperature reaches 338.5 K for SOI device and 331.7 K for MOS transistor. On the other hand, the impact of convective resistances of $R_{th}^{-1}=10^7$, 10^8 and 10^9 W/m²·K is insignificant due to the heat generated by Joule effect and jump condition at the interface which prevails the effect of Robin condition at the source/drain. In addition, the insulating layer in SOI-MOSFET caused to accumulate heat in the channel, which led to an increase of heat in the channel and thermal instability compared with MOSFET. These simulation findings contribute in several ways to the understanding of the thermal behavior within the nano-transistors under the effect of Robin condition, and they are hoped to help other researchers to understand the thermal transfer mechanism on the one hand meso-scale method. However, it is noted that further research is needed to better understand the influence of Robin condition and the temperature jump boundary condition.

Chapter IV: Investigation of heat conduction in MOSFET device based on Graphene material

IV.1 Introduction

The emergence of nanotechnology has cemented the prompt development of nanoscale transistors based on semiconductor material [86]. In the last few decades, there has been a surge of interest in the effects of phonon heat transfer on nano-transistor performances [87, 88]. The most commonly utilized semiconductor for microelectronic devices was silicon (Si). However, because of the miniaturization to nanoscale, the devices based on silicon are approaching their material limits [17, 55]. The device systems based on graphene material have drawn considerable interest due to its outstanding electrical characteristics such as high hole and electron mobility at low heat and high doping concentration, and its high thermal conductivity [89, 90]. Carbon-based graphene material is included in many applications such as elastic nanoelectronics [91], graphene transistor devices [92, 93], light-emitting diodes [94, 95], and solar cells [96, 97]. Fourier law is significant to the thermal transport process, which suggests that heat transport passes in the diffusive regime. However, it is known that the classical heat conduction equation cannot be applied to the heat transfer in nanoscale structure when the Knudsen number is high (ballistic regime) because the length of the structure reaches the phonon mean free path of materials [98-100]. As a consequence, the thermal characteristics differ remarkably from that of the large bulks [101]. Some theories instead of Fourier law have been developed to describe the thermal behavior in nanostructures, including phonon dynamics [4, 39], thermo-mass theory, and phonon hydrodynamics [102, 103].

On the significance of heat transfer in these silicon material based nanoscale isotropic homogeneous-structure MOS transistors, many macroscopic theoretical studies have been reported [8, 9, 16, 104]. But, because of that the ballistic regime appears at high value of Knudsen number, the material structure of MOSFET becomes anisotropic. This causes a change in the thermal properties and in the effective thermal conductivity [105, 106]. The present work utilized mesoscale theoretical method based on the lattice Boltzmann equation to study the heat transport in graphene nano- transistor and silicon transistor considering the effects of effective thermal conductivity and TJBC. In the analysis of thermal transfer within the nanostructures, the model proposed is considered an efficient approach opposed to macroscopic methods. This is because the material medium is sub-continuous in the existence of particle movement [3, 43].

IV.2 Two-dimensional analysis of heat conduction

In general, particle vibration (phonon) limits the thermal transfer within a nanoscale domain where the decrease in dimension of structure to the mean free path of material with phonon scattering at boundary influences the heat conduction process [107]. The bulk based on thermal conductivity is modeled by the solution of the phonon Boltzmann transport process model where the ETC is related to the Knudsen number [108]. Hence, the length-dependent ETC across the channel device system can be expressed as [53, 55, 105]:

$$k_e(Kn) = k\left[1 - \frac{2\times Kn\times \tanh(1/(2\times Kn))}{1 + c_p \times \tanh(1/(2\times Kn))}\right] \quad \text{(IV.1)}$$

Here c_p and Kn are the constant linked to the characteristic of the material and the Knudsen number, respectively, while c_p = 2(1+p)/(1-p) where p being the specularity parameter determined as a probability of phonon scattering process at the boundary [68, 109]. In addition, the relaxation time associated to the phonon scattering at the boundary is defined as [53, 64]:

$$\tau_b = \frac{3\times k_e}{C\times v^2} \quad \text{(IV.2)}$$

In this case, Eq.(II.5) stated as fellow:

$$\frac{\partial u}{\partial t} + v.\nabla u = -\frac{u - u^{eq}}{\tau_b} + q_v \quad \text{(IV.3)}$$

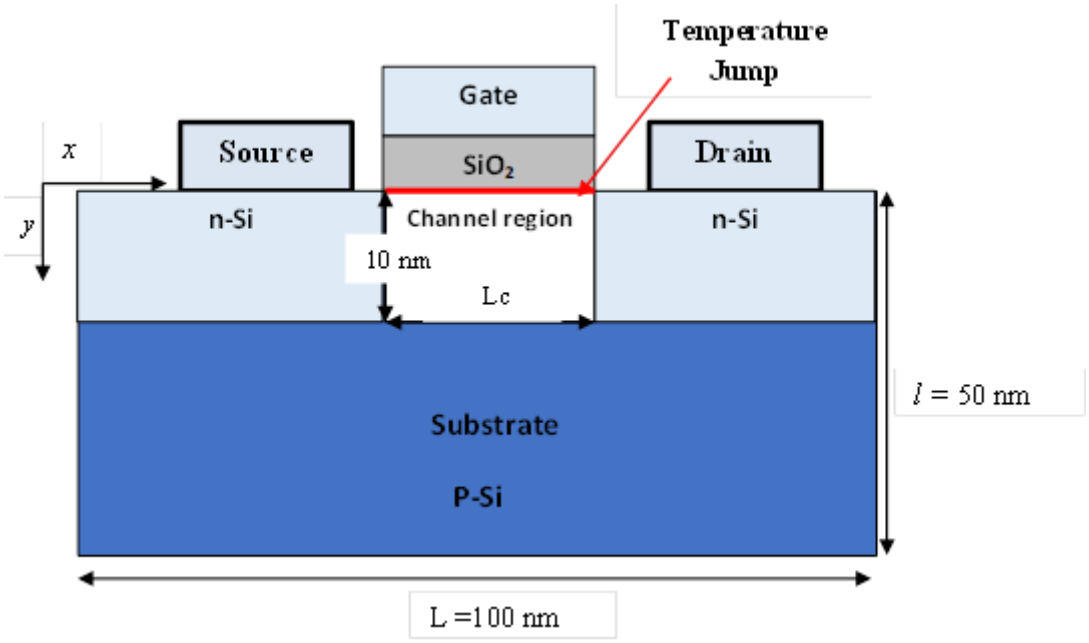
Thus, Eq. (IV.3) can be expressed in non-dimensional form as:

$$u_i^*(x^* + \Delta r^*, t^* + \Delta t^*) - u_i^*(x^*, t^*) = -\frac{\Delta t^*}{\tau_b^*}\left[u_i^*(x^*, t^*) - u_i^{eq*}(x^*, t^*)\right] + w_i q_v^* \quad \text{(IV.4)}$$

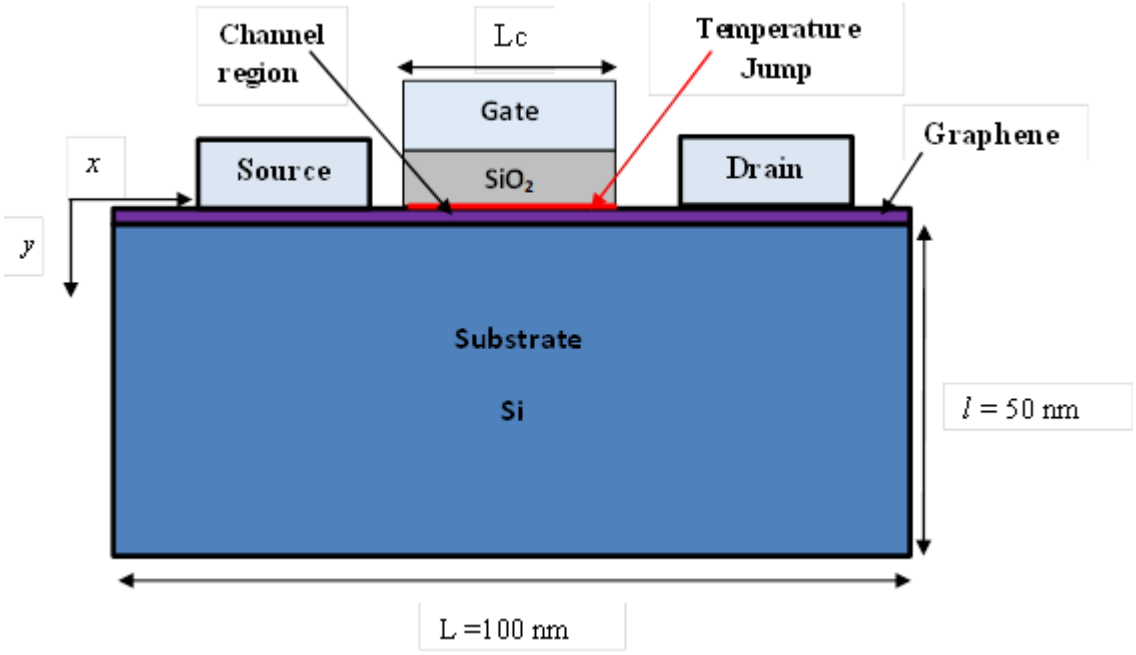
IV.2.1 Description of structure

A graphene (Gr) MOS transistor consists of a gate, an oxide layer and a graphene layer channel electrically connected to the source electrode and the drain electrode [110, 111]. For the study suggested by the mesoscopic method, the simulation designs are portrayed in FigIV.1 and IV.2. FigIV.1 shows the structure of a traditional Si-MOS transistor device. The sizes of device considered in this work are L=100 nm and l =50 nm with a heat generation area is L_c×10 nm. The geometry of the simulated Gr-MOSFET is given in Fig IV.2 where the thickness of graphene

nano-ribbon is 0.35 nm [67] which is placed between the silicon and the oxide [111]. A constant heat generation in the active channel of nano-transistors is presumed (q_v=10^{19} W/m^3). For the numerical simulation in this study, the utilized heat characteristics of materials are mentioned in Table IV.1.



FigIV.1: A schematic representation of Si- MOSFET.



FigIV.2: A schematic representation of graphene(Gr)- MOSFET.

TableIV.1: Heat features of Silicon dioxide (SiO_2), Graphene (Gr) , and Silicon (Si) [68, 112]

/	v (m s^{-1})	k (W. $m^{-1}K^{-1}$)	Λ (nm)	C (J. m^{-3} K^{-1})
Si	3000	150	100	1.5×10^{6}
Gr	14740	4000	518	1.57×10^{6}
SiO_2	5900	1.4	0.4	1.75×10^{6}

IV.2.2 Boundary conditions

The boundaries are supposed to be adiabatic at the top, right side, and left side of both MOS transistors. Besides, the bottom boundary is assumed to be at a uniform temperature of 300 K. The initial temperature of all point locations of the nanodevices is considered at 300 K. At the semiconductor-oxide interface, the jump condition is connected to the oxide-gate [9, 16], the TJBC is imposed. As previously mentioned, this boundary state defines transistor wall-phonon collisions and is described as follows [10, 82, 104]:

$$T^{*} - T_{w}^{*} = -a \times Kn \times L_{c}^{*} \frac{\partial T^{*}}{\partial y^{*}} \tag{IV.5}$$

where T_w^*, and y^* are the dimensionless temperature of walland the dimensionless direction vertical, respectively, while a represents an adjustable coefficient defined as [68, 113]:

$$a = \frac{\mathrm{R}_{cont} \times k_e}{Kn \times L_c} \tag{IV.6}$$

where R_{cont} is the interface thermal resistance which is reached 0.9×10^{-9} $m^2\cdot K\cdot W^{-1}$ for Si/SiO_2 interface [114] and 4×10^{-8} $m^2\cdot K\cdot W^{-1}$ for Gr/SiO_2 interface [115].

IV.2.3 Simulation and discussion

In the current work, a 2D heat transport within nano-transistors systems silicon-MOSFET and graphene-MOSFET for the length channel region of L_c =10 nm with the impact of effective thermal conductivity at p=0.5 is reported employing the lattice Boltzmann equation coupled with

TJBC type. The thermal behavior simulation performed in this work was achieved in fortran language with an adopted LBM approach and yielded results are displayed by Tecplot software.

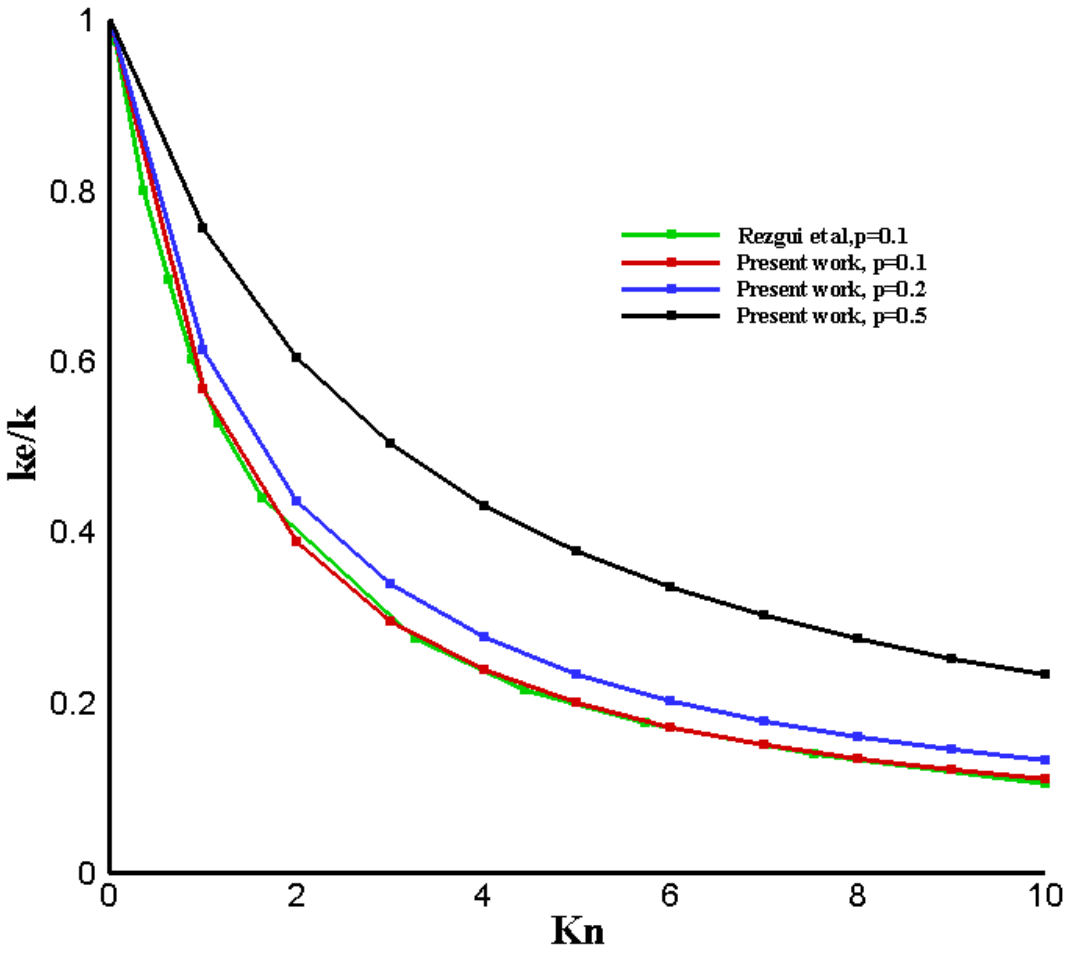
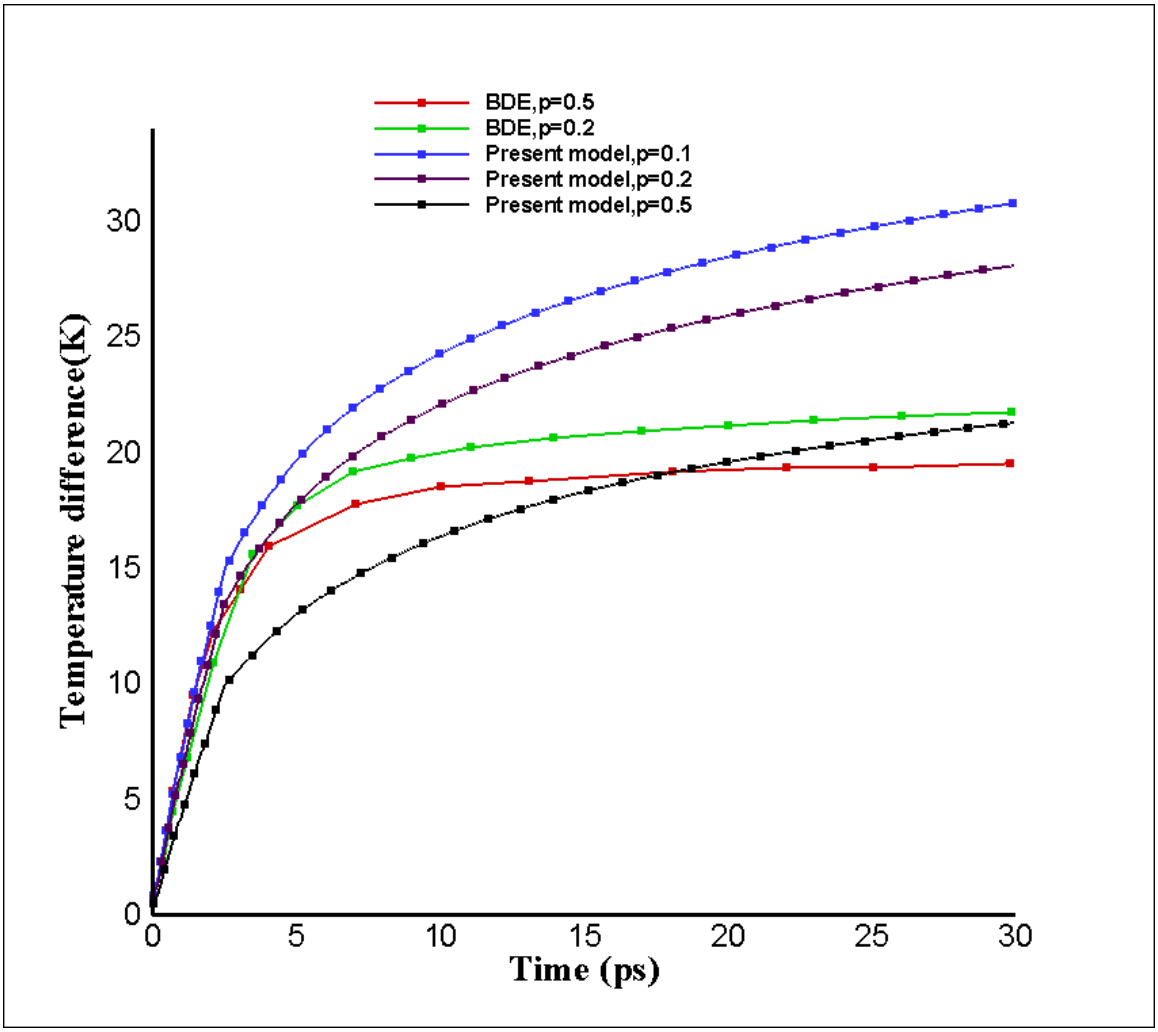


Fig IV.3: The effect of the Knudsen number with different specularity parameter on rapport of thermal conductivity in silicon

Fig IV. 3 presents the effect of the Knudsen number with the specularity parameter on proportion of thermal conductivity in silicon layer which used Eq. (IV.1) to predict the ETC. It is clear that the ETC reduces when the Knudsen number increases. For p=0.1, the result of present work is in agreement with Rezgui et al. [53]. Furthermore, the effective thermal conductivity augments when the specularity parameter increases as shown in p=0.2 and 0.5.

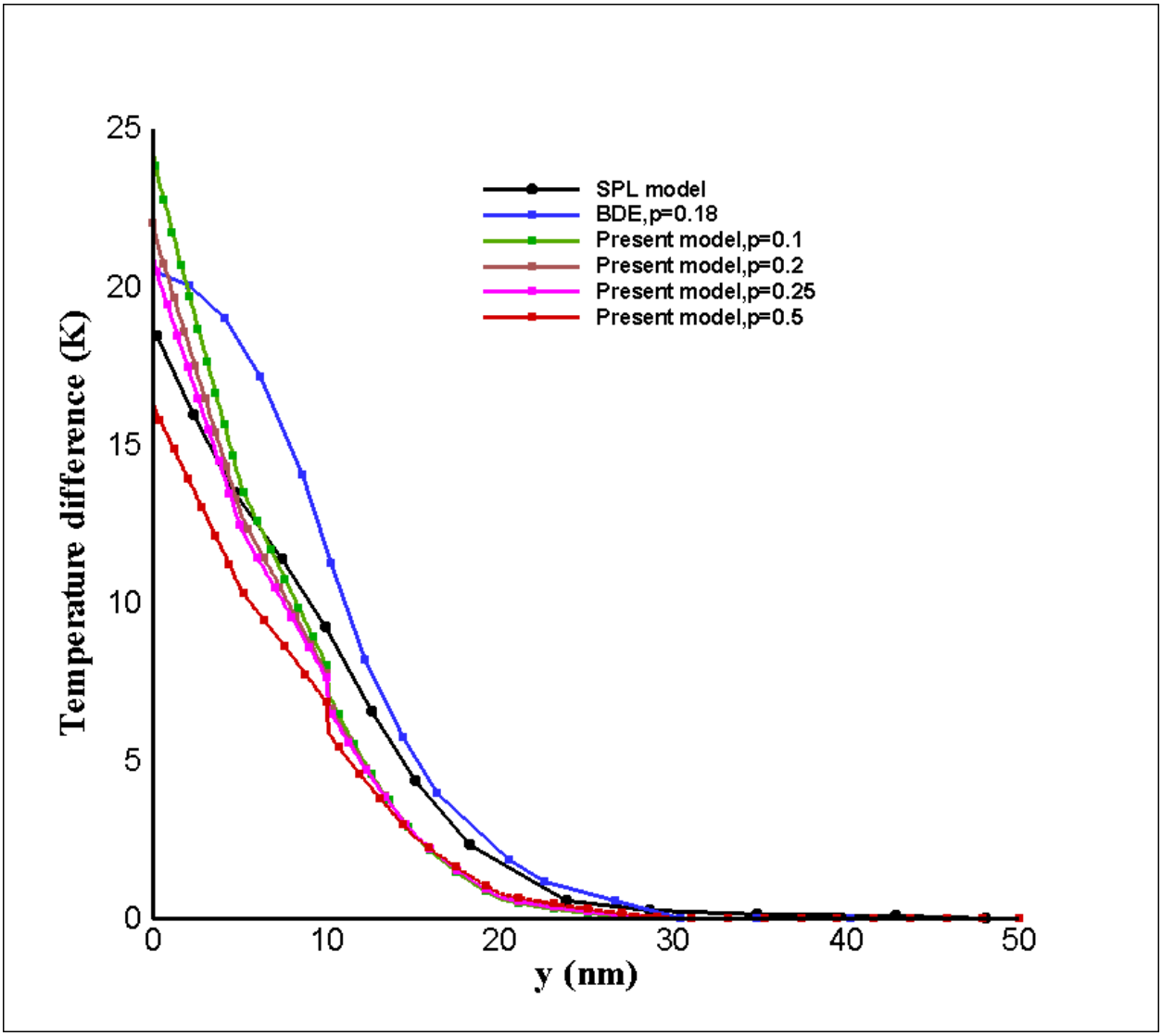
To verify the proposed LBM model for the evolution temporal of temperature at (L/2, 0), a comparison of the outputs of the suggested model is made with those of the BDE model [68]. The evolution of the peak temperature rise (T-T_{ref}) in the centerline of the zone on Si-MOS nano-transistor is plotted in FigIV.4. Comparison of these two models show the temperature elevation



FigIV.4: Evolution temporal temperature difference of Si-MOSFET

when the specularity parameter reduces due to the decrease in the ETC. In addition, the results of peak temperature trend are in agreement with those obtained by BDE model. The difference in the temperatures values are due to the different method used.

Fig IV.5 illustrates the temperature difference along the *y*-axis at the centerline in the nano-Si transistor. The temperatures values in the SPL model [9], BDE model [53], and the present



FigIV.5: temperature profiles along y-direction in the centerline of Si- MOSFET with the present model, SPL, BDE at t = 10 ps .

model (y >20nm) are similar. In the model suggested, the maximal temperature at the connect Si-SiO_2 is close to those of the BDE model at the specularity of p=0.2 and 0.25. The reduction of ETC and the increasing of phonon scattering process at the Si-SiO_2 interface leads to growing of heat generation across the channel zone. The temperature profile declines when the specularity parameter increases as can be seen by comparing the results of p=0.1 and 0.5. Furthermore, the

present findings show that the specularity parameter improvement causes a significant enhancement in the thermal stability since the suggested boundary condition characterizes the interfacial thermal transfer.

Comparison of temporal temperature difference in the zone $x = L/2$, $y = 0$ of silicon-MOSFET and Gr-MOSFET is presented in Fig.IV. 6 for p=0.5. The hotspot increases with elapsed time. At time scale t=50 ps, it is clear that the nanotransistor, which depends on graphene material in

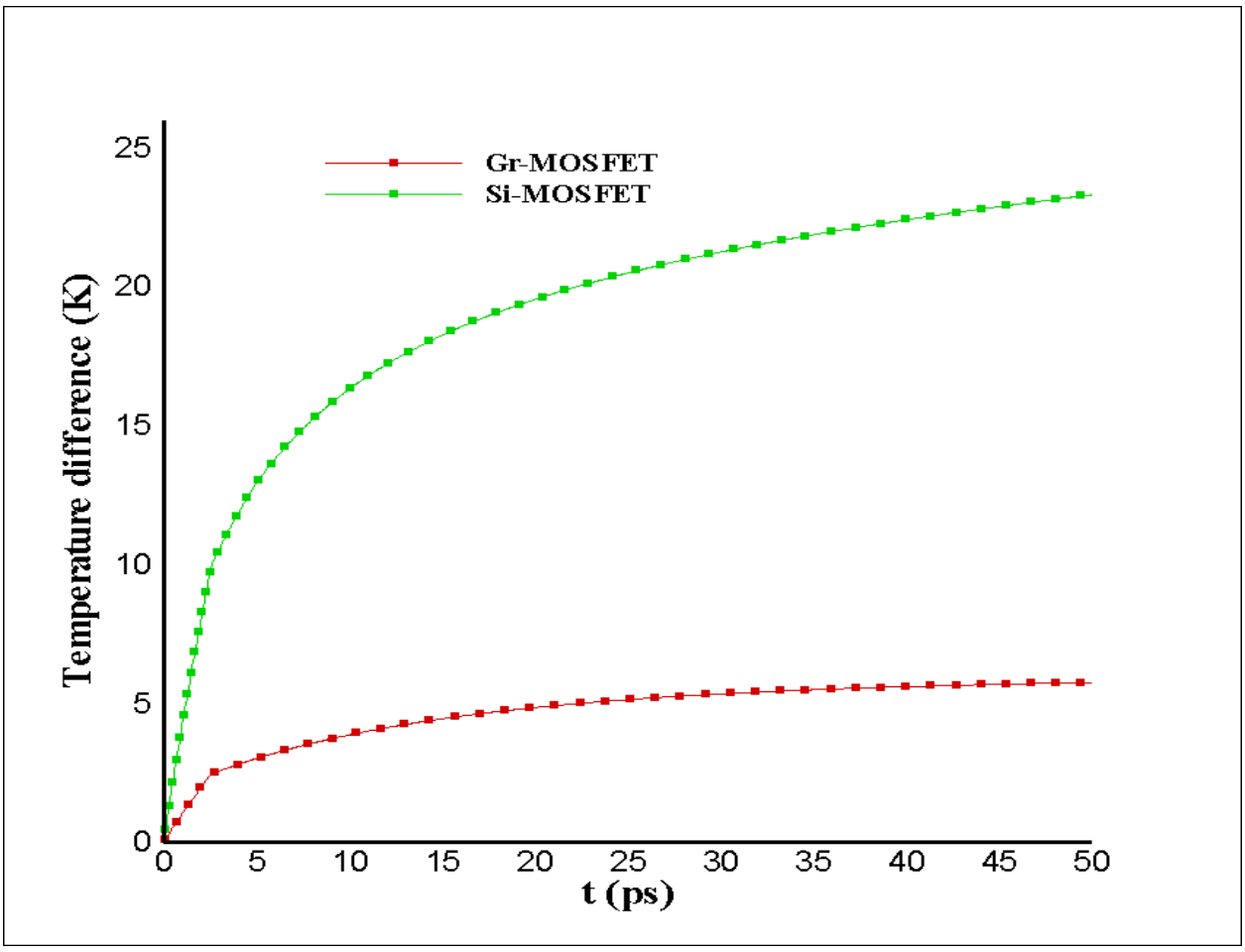


Fig.IV.6: Evolution temporal temperature difference of Si-MOSFET and Gr-MOSFET at $x=L/2$, $y=0$ (p=0.5)

manufacture, is thermally more stable than the material of silicon where the temperature estimates 5.7 K for the graphene transistor and 23.2 K for the silicon transistor. The temperature

difference between these nanodevices reaches 17.5 K due to larger thermal conductivity of graphene, compared with silicon.

Fig IV.7 shows the evolution of the distribution of temperature difference versus *y*-axis in centerline x = L/2 of silicon and graphene transistors at different times ranging from 10 ps to 50 ps. The maximal hotspots are located at the interface for both nanodevices. However, it is

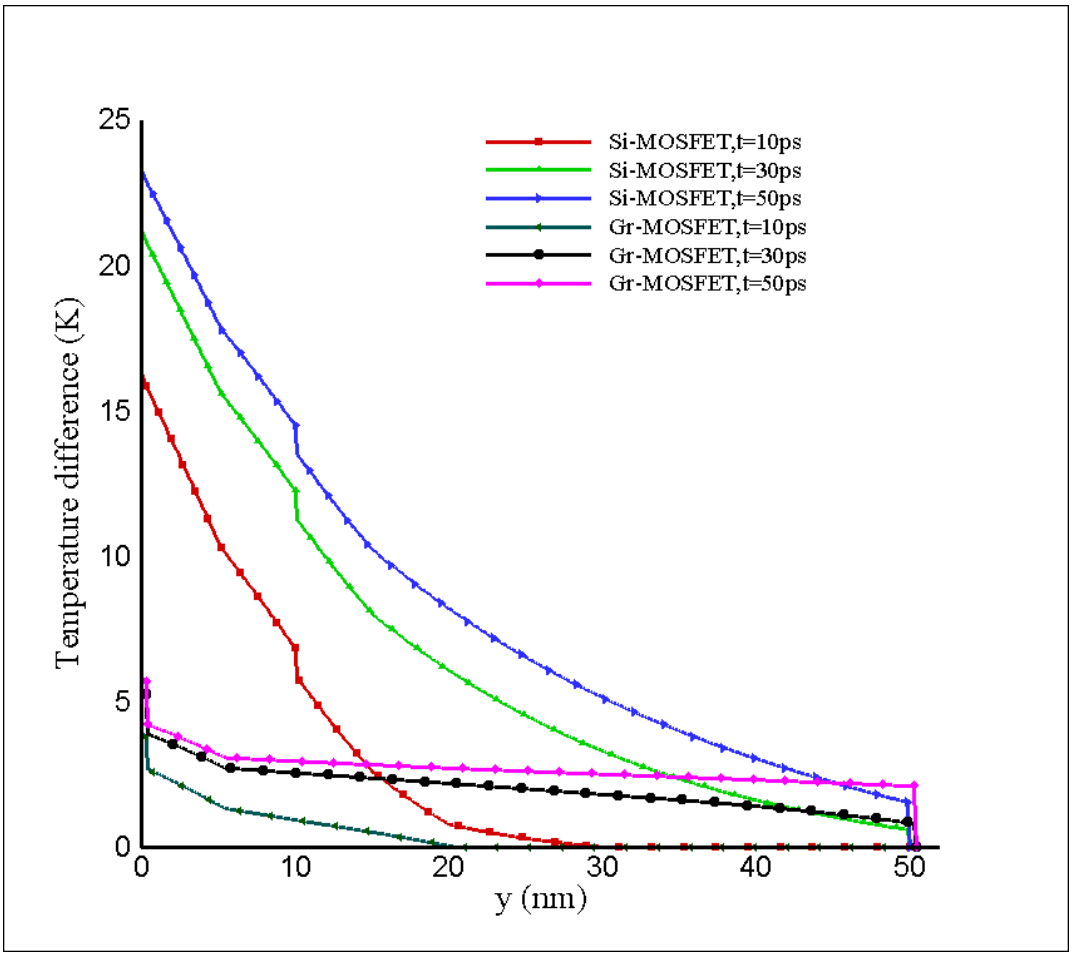


Fig IV.7: Peak temperature versus *y*-axis of the Si and Gr-transistors for different times.

noticed that in the Si-transistor, the hotspot has a greater value than that gained within the Gr-transistor. The variation of peak temperature in the interface due to collision phonon-wall is more frequent with time and it is related to the relaxation time. At t=30 ps and 50 ps, because of the high Knudsen number in the substrate (the ballistic phonon transport), the temperature drops sharply at the bottom of the nanodevice.

Fig IV.8 represents a comparison of temperature versus *x*-direction of nano transistors in *y*=0 for different times. The form of the curves is symmetric in regard to the centerline axis. It is apparent from the results that the maximum hotspot is located at centerline and it grows with elapsed time

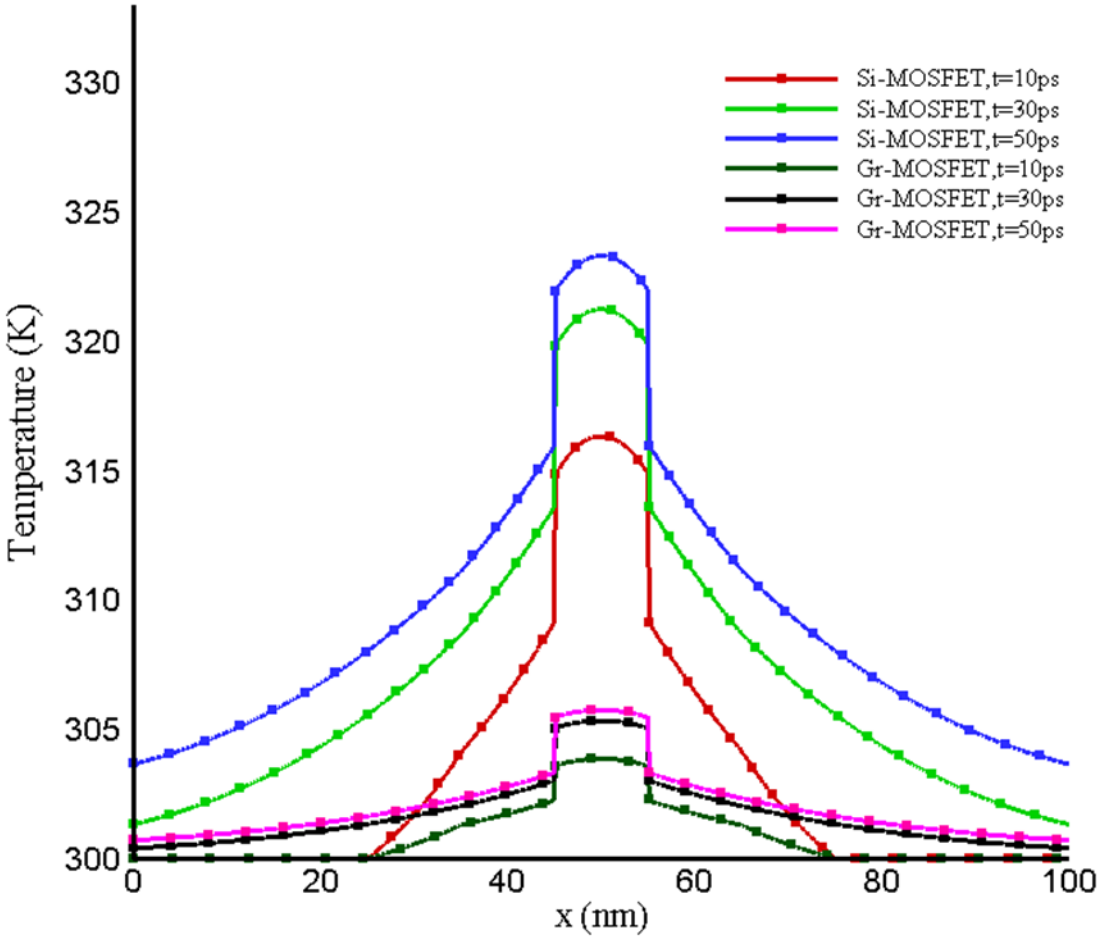
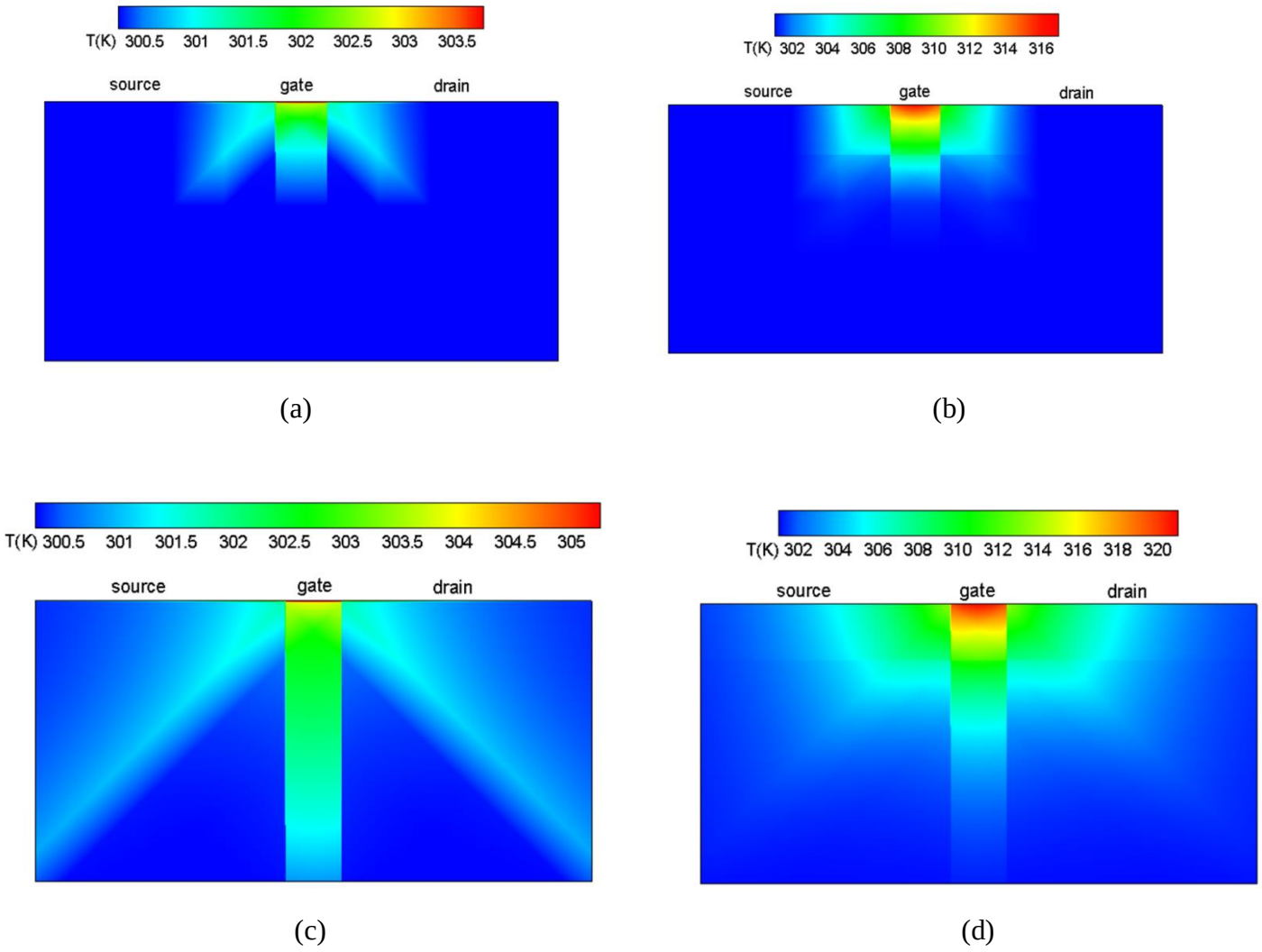


Fig IV.8: Evolution temperature versus x-axis of the Si-MOSFET and Gr-MOSFET at y = 0.

and remarkable hotspots exist at the active region because of the generated heat as a result of Joule effect (electron-particle) and collision on the interface of wall-phonon. In silicon transistor, the maximal temperatures reach 316.3K, 321.2K, and 323.2K at 10 ps, 30 ps, and 50 ps, respectively, whereas in the graphene transistor lower maximal temperatures are registered, 303.8 K, 305.3 K and 305.7K corresponding to 10 ps, 30 ps, and 50 ps, respectively. This difference in the maximal hotspots is due to the lower thermal conductivity of the silicon material compared with graphene which has high thermal conductivity.

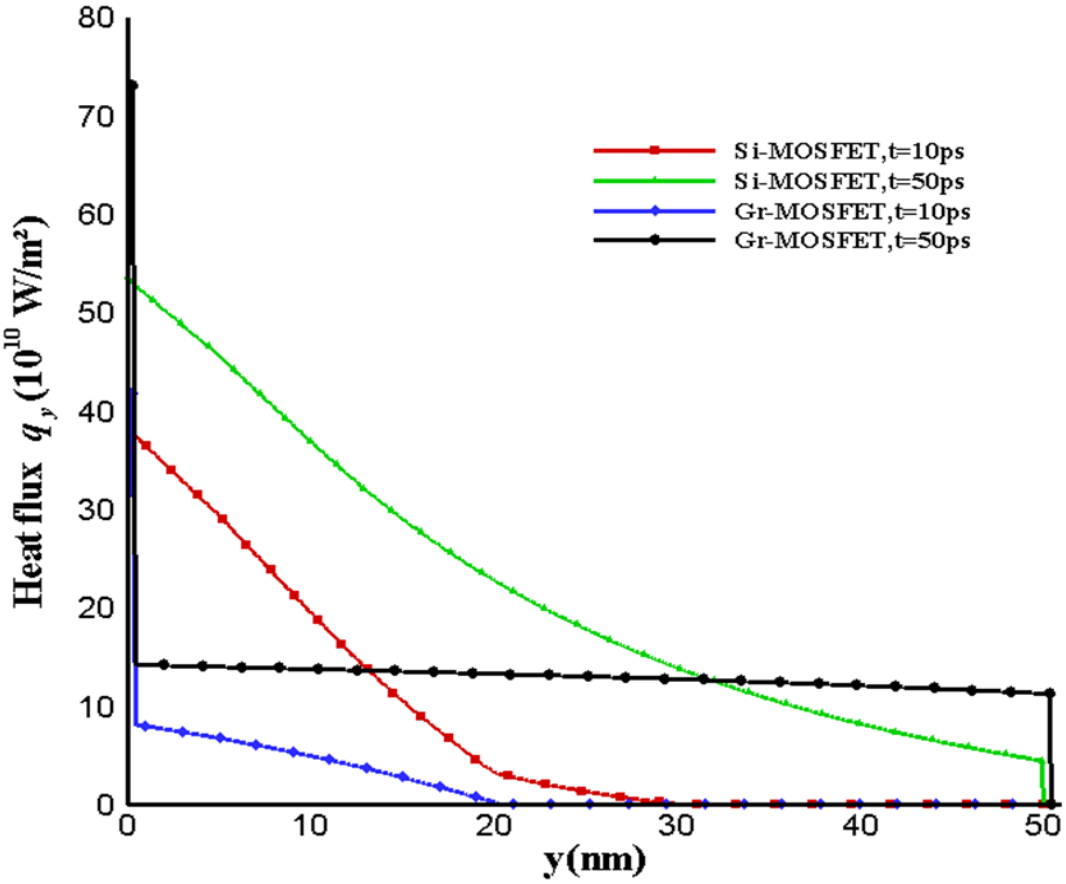
FigIV.9 exhibits a 2D distribution of thermal behavior within Si/Gr MOS transistors at *t*=10 ps and 30 ps. The figures confirm the previous results, i.e. the high hotspots are located in the active zone. It can be seen that the heat conduction occurs on the left side, right side, and bottom of the



FigIV.9: 2D evolution temperature distribution with time in Si-device at: b) 10 ps ,d)30 ps and in Gr-device at: a) 10 ps ,c)30 ps

active channel in both nano-transistors. In addition, the results indicate that there is a clear trend of increasing heat conduction spreads to the bottom of transistors at a rapid pace over time because of the low isothermal temperature and the domain space being smaller than the average free path of material.

Fig.IV.10 shows the profile of heat flux along the *y*-direction in the centerline ($x=L/2$) of both nanodevices obtained at t = 10 ps and 50 ps. From this graph, it can be seen that the heat flux in the graphene nano-sheet of Gr transistor is higher than the Si transistor at the interface for various times, because the graphene device are destined to afford the increase of thermal removal due to its high thermal conductivity [89]. The estimated maximal heat flux at t=10 ps and 50 ps is respectively 42.3×10^{10} and 73.7×10^{10} W/m² for the graphene nano-device, on the other hand, it is 38.4×10^{10} and 53.5×10^{10} W/m² for the Si MOS transistor.

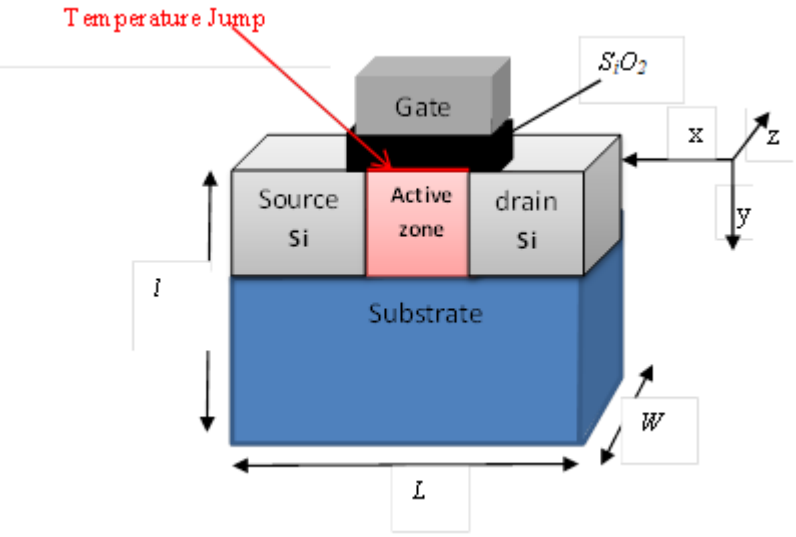


FigIV.10: Heat flux profiles along *y*-axis of the Si and Gr-transistors for different times at x=L/2.

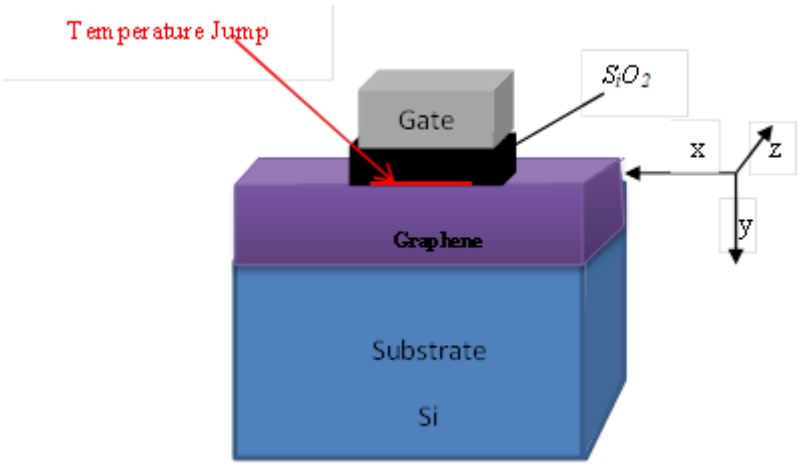
IV.3 Three-dimensional analysis of heat conduction

IV.3.1 Description of structure

The thermal behavior simulation performed in this work was achieved with an adopted LBM approach written in Fortran language and yielded results are displayed by Tecplot software. The simulation designs for the study proposed by the meso-scale approach are seen in FigsIV. 11 and IV.12. FigIV.11 represents a size of a Si-device structure. The size of component under consideration in this study is l =50 nm, L=100 nm and W=1µm with a volume of heat source is 10 nm×10 nm×1000 nm. Fig.IV.12 represents the size of a graphene field effect transistor device, this device includes few layers of graphene thickness of 4 nm. A constant heat generation in the active channel of nano-transistors is presumed (q_v=10^{19} W/m^3).



FigIV.11: Schematic of Si-MOSFET device



FigIV.12: Schematic of Gr-FET device

IV.3.2 Boundary conditions

The boundaries are supposed to be adiabatic at all boundaries of both MOS transistors. Besides, the bottom boundary is assumed to be at a constant temperature (300 K). The initial temperature of all point locations of the nanodevices is considered at 300 K. The jump condition is connected to the oxide-gate [9, 16, 65, 66], i.e. TJBC is imposed. As previously mentioned, this kind of boundary defines device collisions wall-phonon .

For the modeling of heat transport phenomena, several models of the Lattice Boltzmann technique have been presented, which can give adequate accuracy for high Knudsen number values [10, 66, 84, 116]. For the heat conduction, a three-dimensional (3D) simulation is conducted with a lattice for D_2Q_{15} model describes the discrete points arranged [77].

The isothermal boundary condition at the bottom of devices is described as [65, 77]:

$$u_i^*(x^*,m,k)=\frac{u^*(x^*,m,k)}{15} \qquad \text{i} = 0...14 \tag{IV.7}$$

Adiabatic boundary condition is applied at all other boundaries, which can be treated as follows [10, 65]:

$$\begin{aligned} &u_i^*(0,y^*,z^*)=u_i^*(1,y^*,z^*)\\ &u_i^*(n,y^*,z^*)=u_i^*(n-1,y^*,z^*) \quad \text{i} = 0..14\\ &u_i^*(x^*,0,z^*)=u_i^*(x^*,1,z^*)\\ &u_i^*(x^*,y^*,0)=u_i^*(x^*,y^*,1)\\ &I_i^*(x^*,y^*,k)=I_i^*(x^*,y^*,k-1) \end{aligned} \tag{IV.8}$$

For the current model, the jump condition (TJBC) at the top is treated as [66] :

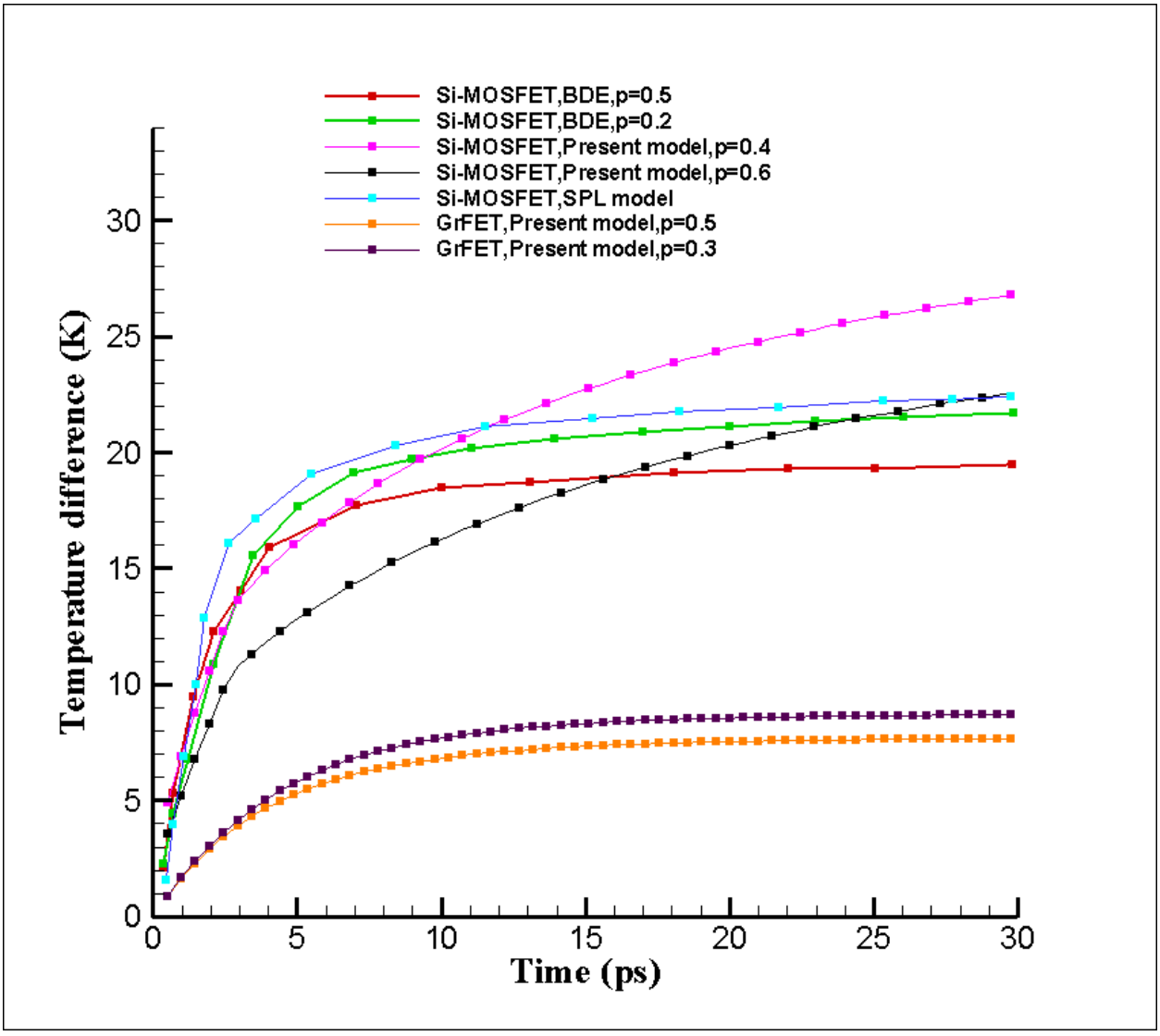
$$u_i^*(x^*,0,z^*)=\frac{\frac{\Delta y^*}{L_c^*}\frac{u_w^*}{15}+a.Kn.u_i^*(x^*,1,z^*)}{\frac{\Delta y^*}{L_c^*}+a.Kn} \qquad \text{i} = 0..14 \tag{IV.9}$$

IV.3.3 Simulation results and discussion

In the present investigation, thermal conduction inside 3D silicon and graphene nano-devices for the length channel region of 10 nm with the impact of specularity parameter and effective thermal conductivity are reported employing the lattice Boltzmann equation coupled with TJBC type. The interface thermal resistance is 0.9×10^{-9} $m^2\cdot K\cdot W^{-1}$ for the Si/SiO_2 interface [114] and 4×10^{-8} $m^2\cdot K\cdot W^{-1}$ for the Gr/SiO_2 interface [115].

The temporal distribution of temperature in the Si-MOSFET and Gr-FET at the centerline is displayed in FigIV.13.To verify our numerical model, we first compared our results for Si-transistor device with those obtained by BDE model [68] and SPL model [9]. It is abundantly

evident from the figure that that all models permit the same path for the growth in temperature difference (T- T_{ref}). The increase in the specularity parameter has a positive effect on lowering the temperature at the interface because of the augmentation in the effective thermal conductivity, which affects the phonon collision rate and leads the peak temperature rise in the silicon device to reach 26.7 K for p=0.4 and 22.5 K for p=0.6. Also, we can see the same influence (specularity) inside the graphene device where the peak temperature is 8.7 K and 7.8 K for p = 0.3 and 0.5, respectively.



FigIV.13: Comparison of the temporal temperature difference in the centerline of the nano-transistors

The comparison of temperature difference along the y-direction at the centerline of the low-dimensional devices at time scale t = 10 ps is demonstrated in FigIV.14. In Si-device, our present

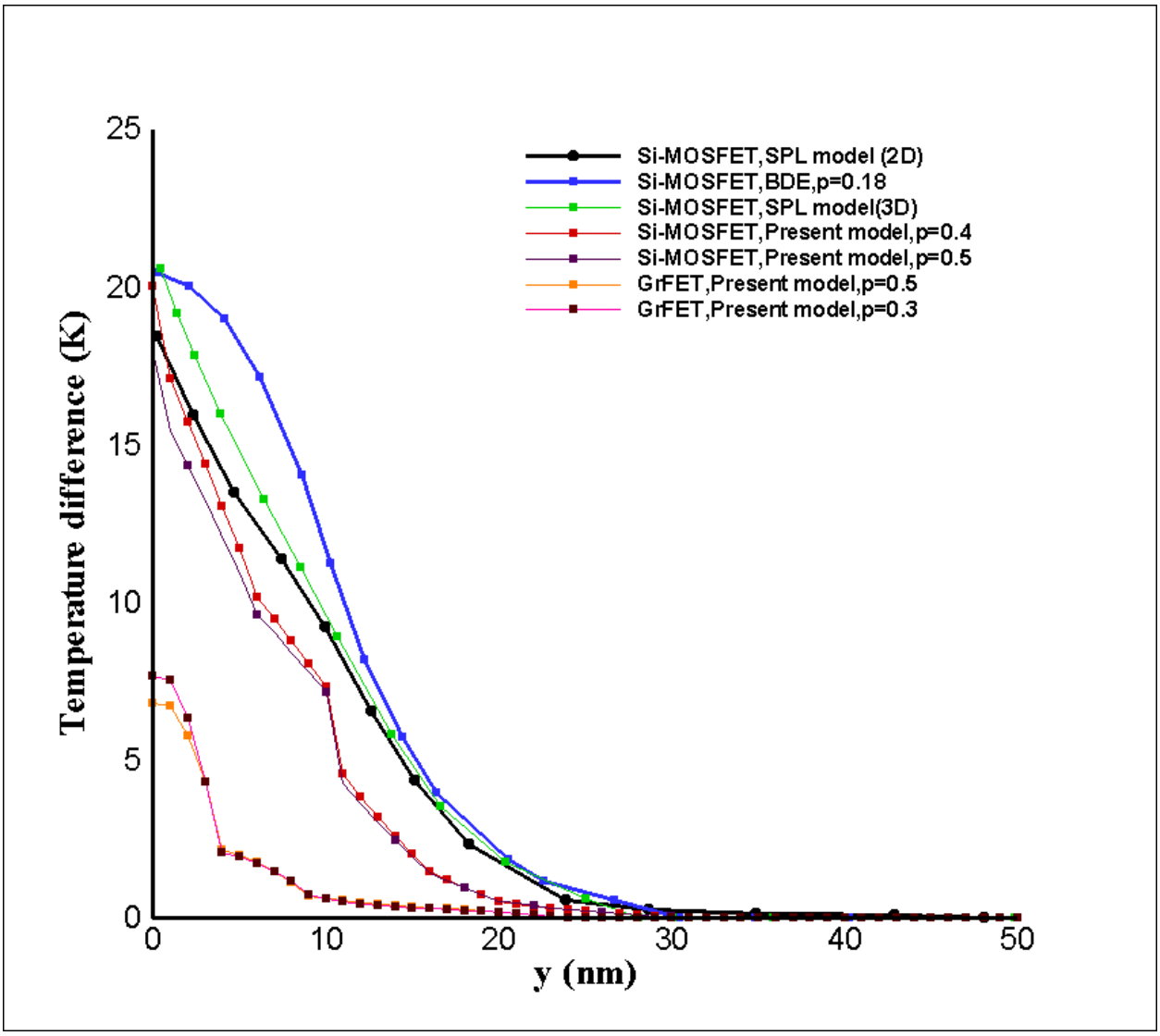
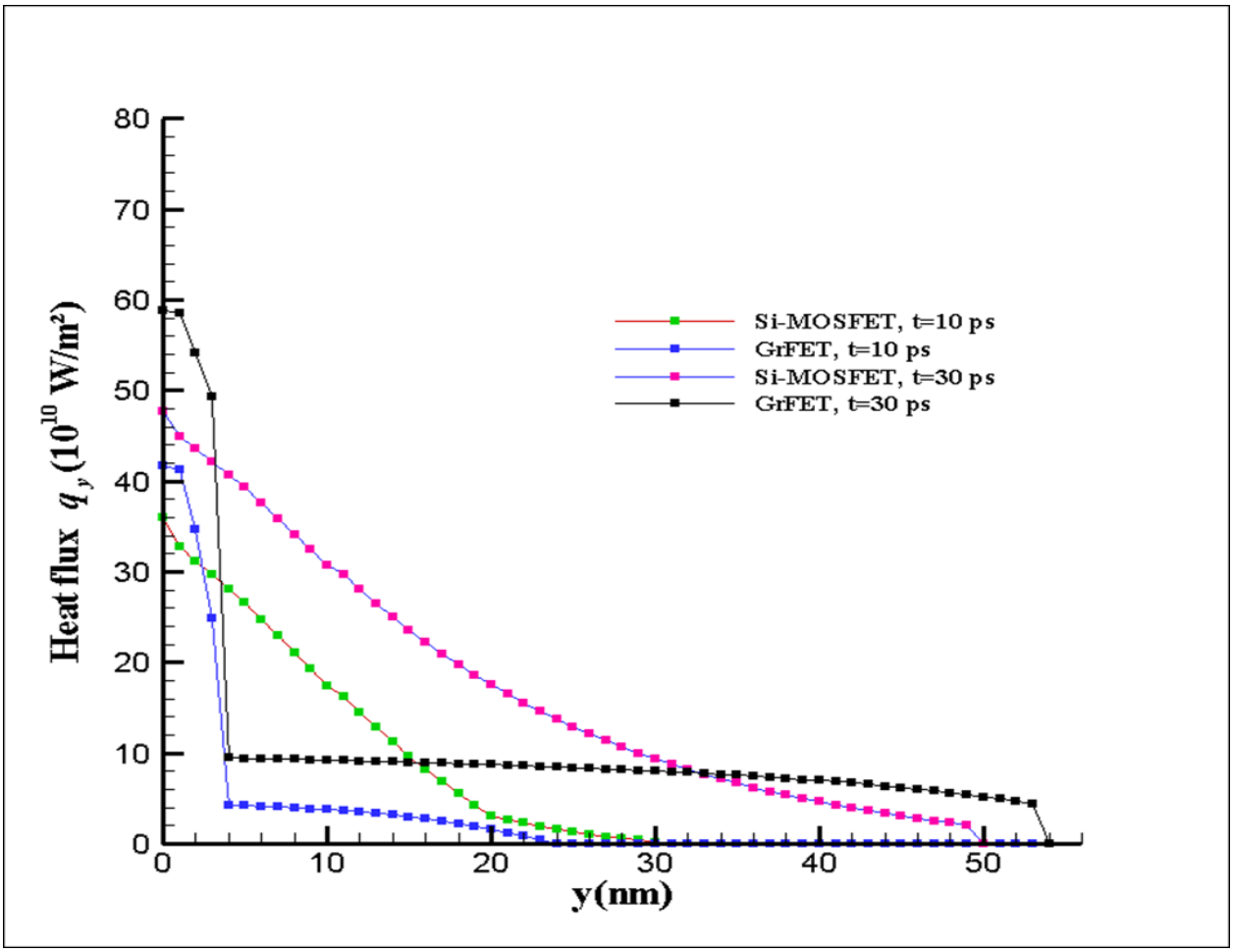


Fig.IV.14: Comparison of temperature profiles in the centerline of the nano-devices at time scale t =10 ps

model has the same trend as SPL model in [9] and BDE model in [53] in the nano-structure device, the maximal temperature is close to the heat zone due to the heat generated. The temperature decrease is owed to the decrement in the thermal conductivity. Due to the collision rate, which depends on the specularity, the difference is more profound in the low temperature. For p = 0.6 and p = 0.4, the predicted maximum peak temperatures are respectively 16.1 and 20 K. On the other hand, due the high thermal conductivity of the graphene material, the peak temperature is declined in Gr-FET device compared with the transistor based on silicon material.

The temporal heat flow versus y-direction in the centerline of the silicon and graphene devices is presented in FigIV.15. It is evident from our model that the heat flow profiles in the active zone have similar shapes but different amplitudes. The maximal heat flow reaches 35.8×10^{10} and

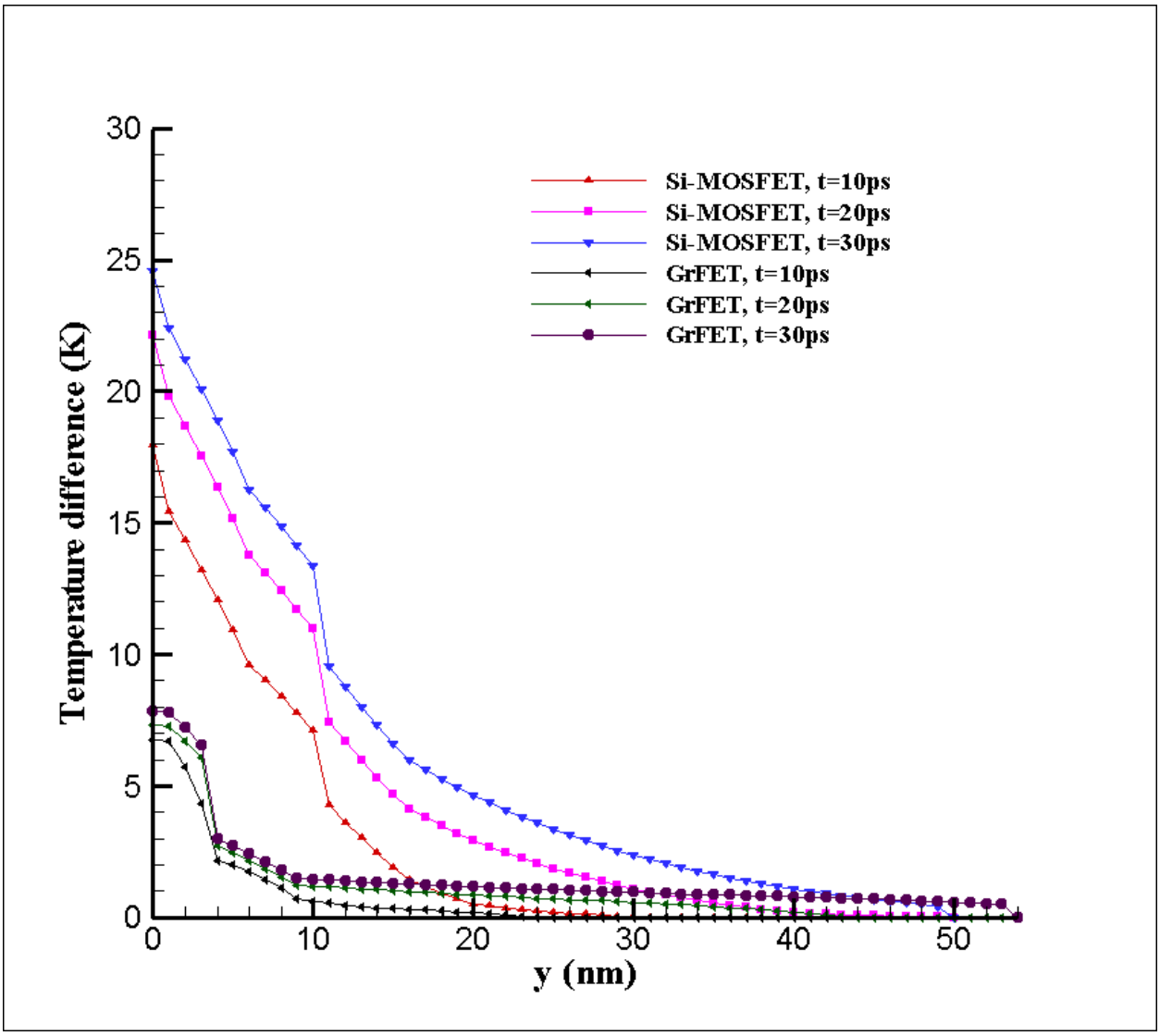


FigIV.15: Heat flux profile versus y-direction in the centerline of transistors at different times and p = 0.5.

47.7×10^{10} W/m^2 in Si-MOSFET at time scale t=10 and 30 ps, respectively. Moreover, the heat flow is estimated 41.6×10^{10} and 58.8×10^{10} W/m^2 in the graphene FET at t= 10 and 30 ps, respectively. This difference in the heat flow is caused by the high thermal conductivity of graphene that helps to extract and exchange thermal energy in a large amount. Also, at t = 10 ps, the heat flow disappears on the substrate side, but at t = 30 ps it has an augmented value. This

divergence is caused by the propagation term and collisions of phonon-wall throughout the transistor, which is plainly seen when the model is employed.

The temperature variation along y-direction in the centerline of Si-device compared with Gr-FET

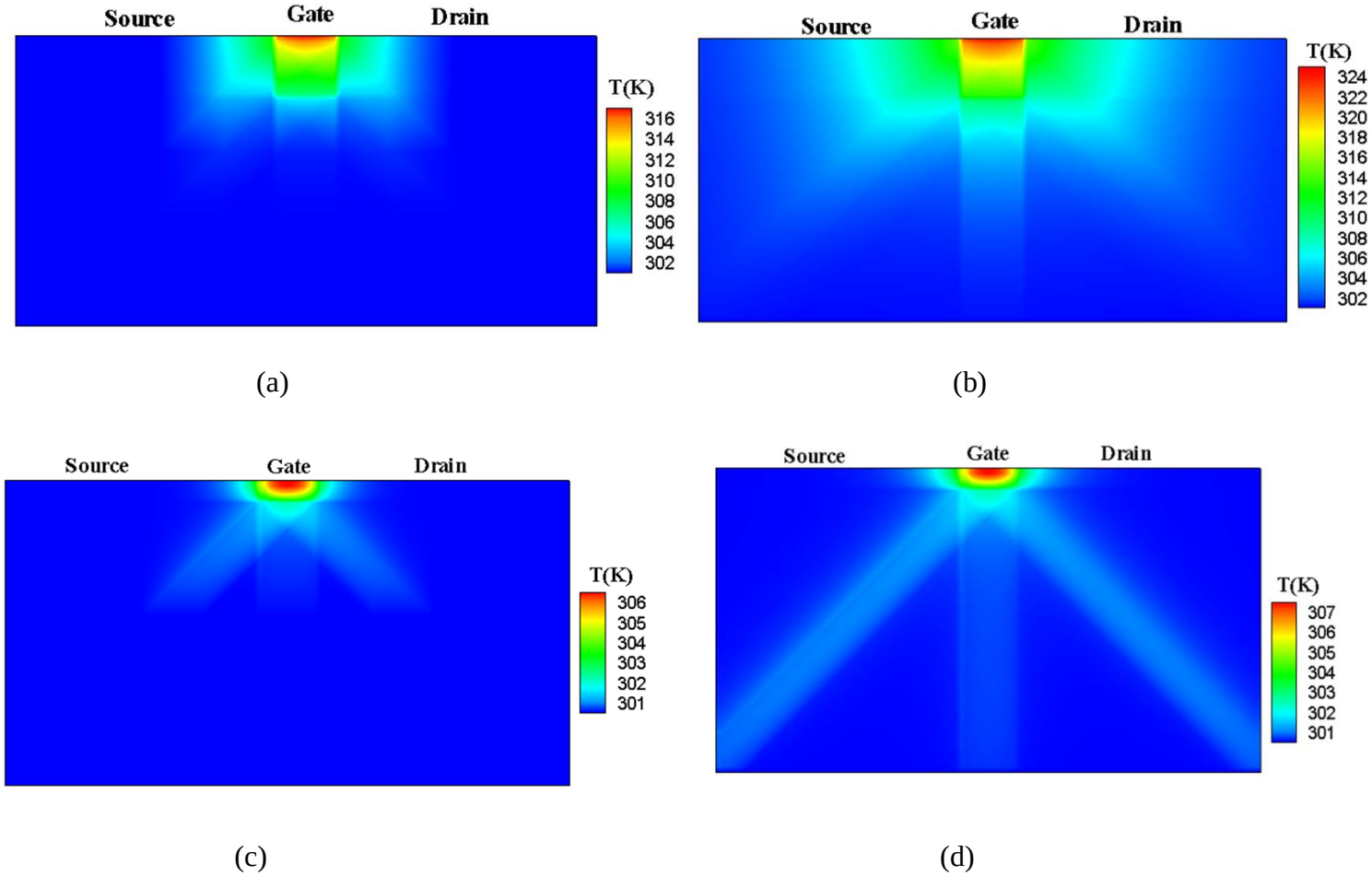


FigIV.16: Temperature difference (T- T_{ref}) profiles versus y-axis of transistors in the centerline at various times and p = 0.5.

at various times t = 10, 20 and 30 ps is plotted in FigIV.16. It is clear that the temperature (T- T_{ref}) has the same trend with various amplitudes and the maximal temperature is located in the oxide-semiconductor interface. This position of the maximum temperature is caused by Joule effect and the collision phonon-wall. It is also noticed that with elapsed time, the region affected by the hotspot enlarges. At t = 10 ps, for example, only the channel region is influenced by the temperature, whereas at t = 30 ps, the entire channel region is affected. In addition, because of

low thermal resistance of graphene, we find that the temperature in devices based on graphene is more stable than its counterpart based on the silicon construction.

The temperature distribution across the x-y direction inside nano transistors at p = 0.5 is represented in FigIV.17. These data clearly exhibit that the hotspot is at its highest in the oxide-semiconductor interface. Also, it is noted that the temperature of the graphene structure device is lower than that of a silicon device. This was demonstrated by the previous results and graphs obtained from the application of present model. The maximal hotspots are estimated 324.5 K in Si-device and 308.7 K in Gr-device at t= 30 ps. It can be shown that the heat diffusion occurs on



FigIV.17: A temperature distribution in x-y plane of nanoscale devices at various times.

For Si-transistor: a) at t = 10 ps, b) at t = 30 ps .

For Gr-FET: c) at t = 10 ps, d) at t = 30 ps.

the left side, right side and bottom of the active zone in nano-transistors. In addition, the results indicate that there is a clear trend of increasing heat transfer spreads to bottom of nanodevices with a rapid pace over time because of the low isothermal temperature and the domain space being smaller than the average free path of material.

IV.4 Conclusion

The purpose of the current work is to investigate the effect of the specularity factor on the heat conduction in nanoscale Si- and Gr-MOSFETs at Lc=10 nm utilizing the lattice Boltzmann equation. The D_2Q_8 model with temperature jump condition have been used for the operating period up to t=50 ps. The suggested work has been proved on the backbone of available results from the previous studies. In general, the simulation results show that the temperature jump which occurs in the interface due to the phonon-wall collision in silicon transistor and graphene transistor causes the maximal heat at the interface where the temperature reaches 305.7K for the Gr-transistor and 323.2K for the Si-transistor. Moreover, due to higher heat flux ability and the low temperature, the graphene transistor is thermally more stable than the Si transistor nanodevices. The specularity parameter and Knudsen number affect the effective thermal conductivity value which results in elevation or decrease of temperature in nano transistors. In addition, the augment of the specularity parameter (p>0.1) enhances the thermal stability of the transistors systems. The preferences of graphene transistor devices and the unique properties of graphene materials makes this material a good candidate for future nano electronics systems generation. Also, we addressed the downscaling three-dimensional heat conduction constraints of conventional Si-MOSFET and Gr-FET devices using the LBM D_3Q_{15} model coupled with influence specularity factor and the temperature jump boundary condition type. The suggested work has been proved on the backbone of available results from the previous studies. The simulation results display that the specularity parameter impacts the effective thermal conductivity value which results in elevation or decrease of temperature in nano-devices. In addition, the augmentation of the specularity enhances the thermal stability of nanoscale transistors systems. At time scale t= 30 ps and p=0.5, the temperature is 308.7K and 324.5K for the Gr-FET and Si-MOSFET, respectively. Meanwhile, the heat flux reaches 47.7×10^{10} W/m^2 in Si-MOSFET 58.8×10^{10} W/m^2 in graphene FET at t = 30 ps. From a theoretical viewpoint, the preferences of graphene devices and the unique proprieties of graphene material make this

material a good candidate for future nanoelectronics systems generation, and the model utilized is proven to be valid in describing the heat behavior in nanostructures devices systems..

General conclusion

The main objective of this work is to study a contribution to the thermo-behavior in nanoscale MOSFET devices. A number of simulation studies were carried out to understand this transport phenomenon using lattice Boltzmann method coupled with jump temperature boundary condition with effect of parameters. The organization of the study can be concluded as: The first chapter is considered an introduction to MOSFET device technology, where it showed the various structures of the device, the development of the device's size, and the various previous thermal studies that were conducted. In second chapter, the choice of Lattice Boltzmann method was based on several points, it is clear mathematical and physical modeling, easy programming, parallelization and high computational efficiency.This method has the ability to integer structure and implementation of the boundary conditions in this geometry.The simulated results with the adopted LBM model presented in third and four chapters.

The simulation results showed that the temperature reaches 339.5 K and 332.4 K for SOI-MOSFET and MOSFET at a Knudsen number of 10, respectively, while the heat flux reaches 21.5×10^{11} W/m^2 for SOI transistor and 18.7 $\times10^{11}$ W/m^2 for MOS device. The insulating layer (SiO_2) in the SOI transistor restrains heat release in the channel region. So, the conventional MOSFET at *Kn* =10 is thermally more stable, compared to SOI-MOSFET. On the other hand, The results indicated that there was a positive relationship between the increasing of inverse thermal resistance (R_{th}^{-1}) and the reducing temperature in the source/drain for both devices while the maximal temperature at the interface semiconductor-wall decreases slightly for $R_{th}^{-1}=10^{10}$ W/m²·K at *t*= 30 ps reaching 331.7 K for MOSFET and 338.5 K for SOI-MOSFET. The effect of heat generated in the active channel is more profound than the effect of Robin condition for $R_{th}^{-1}=10^{7}$, 10^{8}, and 10^{9} W/m²·K at *t* = 10 ps. The most obvious findings to emerge from this study is that Robin boundary condition has a slight impact on heat along the channel region at a short time. In addition, this study identified the effect of layer oxide, which stores the heat between the source and the drain.

Also , The suggested work has been proved by available results from previous studies. The current study found that the interface temperature were 323.2K and 305.7K for the silicon-transistor and graphene-transistor, respectively. The obtained results indicate that the specularity parameter (p >0.1) has an important role in the phonon heat transport and in the reducing of the

maximal temperature in the graphene nanoribbon MOSFET. The preference of graphene device and the unique properties of graphene material make this material a good candidate for future nanoelectronics systems generation. The advantages of graphene transistor devices, as well as the material's unique properties, make graphene a promising candidate for future nano-devices systems. In addition, this method in the current study may provide a good numerical tool for deep studies of heat transport phenomenon in nanostructures.

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Appendix A: Scientific production

International Publications

1. **O. Zobiri**, A. Atia, and M. Arıcı, "Analysis of heat conduction in a nanoscale metal oxide semiconductor field effect transistor using lattice Boltzmann method," Energy Sources, Part A: Recovery, Utilization, and Environmental Effects, pp. 1-15, 2020.
2. **O. Zobiri**, A. Atia, and M. Arıcı, "Study of robin condition influence on phonon nano-heat conduction using meso-scale method in MOSFET and SOI-MOSFET devices." Materials Today Communications 26 (2021): 102031
3. **O. Zobiri**, A. Atia, and M. Arıcı, "A critical evaluation based on Lattice Boltzmann method of nanoscale thermal behavior inside MOSFET and SOI-MOSFET." Microelectronics Journal 115 (2021): 105191.
4. **O. Zobiri**, A. Atia, and M. Arıcı, " A Three-Dimensional Analysis of Heat Transfer Based on Mesoscopic Method in Nanoscale Si-MOSFET and Gr-FET," Superlattices and Microstructures, 2021, 107123
5. **O. Zobiri**, A. Atia, and M. Arıcı, " Mesoscale Investigation of Specularity Parameter Impact on Heat Transport in Graphene Nanoribbon ". Physica E Low-Dimensional Systems and Nanostructures, 2022, 139: 115153

International communications

1. **O.Zobiri,** and A.Atia, 'A State of the Art: Heat Transfer within a MOSFET System', International Pluridisciplinary PhD Meeting, IPPM'20, 1st Edition, February 23-26, 2020, EL Oued, Algeria.

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Analysis of heat conduction in a nanoscale metal oxide semiconductor field effect transistor using lattice Boltzmann method

Oussama Zobiri [a], Abdelmalek Atia [a], and Müslüm Arıcı [b]

[a]LEVRES Laboratory, Faculty of Technology, University of El Oued, El Oued, Algeria; [b]Engineering Faculty, Mechanical Engineering Department, Kocaeli University, Kocaeli, Turkey

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A critical evaluation based on Lattice Boltzmann method of nanoscale thermal behavior inside MOSFET and SOI-MOSFET

Oussama Zobiri [a], Abdelmalek Atia [a,*], Müslüm Arıcı [b]

[a] University of El Oued, LEVRES Laboratory, Faculty of Technology, 39000 El Oued, Algeria
[b] Kocaeli University, Engineering Faculty, Mechanical Engineering Department, 41001 Kocaeli, Turkey

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Study of robin condition influence on phonon nano-heat conduction using meso-scale method in MOSFET and SOI-MOSFET devices

Oussama Zobiri [a,*], Abdelmalek Atia [a], Müslüm Arıcı [b]

[a] LEVRES Laboratory, Faculty of Technology, University of El Oued, 39000 El Oued, Algeria
[b] Mechanical Engineering Department, Engineering Faculty, Kocaeli University, 41001 Kocaeli, Turkey

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Physica E: Low-dimensional Systems and Nanostructures

journal homepage: www.elsevier.com/locate/physe

Mesoscale investigation of specularity parameter impact on heat transport in graphene nanoribbon

Oussama Zobiri [a,*], Abdelmalek Atia [a], Müslüm Arıcı [b]

[a] El Oued University,LEVRES Laboratory, Faculty of Technology, 39000, El Oued, Algeria
[b] Kocaeli University, Engineering Faculty, Mechanical Engineering Department, 41001, Kocaeli, Turkey

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Superlattices and Microstructures

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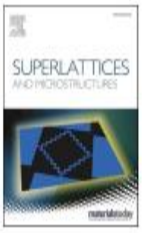

A three-dimensional analysis of heat transfer based on mesoscopic method in nanoscale Si-MOSFET and Gr-FET

Oussama Zobiri [a,*], Abdelmalek Atia [a], Müslüm Arıcı [b]

[a] LEVRES Laboratory, University of El Oued, Faculty of Technology, 39000, El Oued, Algeria
[b] Mechanical Engineering Department, Engineering Faculty, Kocaeli University, Umuttepe Campus, 41001, Kocaeli, Turkey

Appendix B: Indexing of Materials Today Communications

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