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# FPGA Based Implementation of the Sinusoidal Pulse Width Modulation (SPWM)

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**Abstract**

The PWM (pulse width modulation) technique is the result of the recent development in the power electronic domains; it is the heart of the control of static converters. In the present work we propose a hardware implementation using XSG of the SPWM used for three-phase inverter connected to an RL charge. The main purpose is to verify the THD harmonic rate and the resources consumption on FPGA devices. I order to ensure a co-simulation; we firstly used a software simulation of the command part and the used static converter using Matlab/Simulink. Secondly, we convert the same command part using the Blockset added by XSG. Finally we compare the obtained results. XSG is used also to self-generate of synthesizable HDL code for Xilinx-FPGA. The synthesis results are analyzed and compared.

***Keywords*:** Hardware implementation, PWM, System-Generator, voltage source converter, medium-voltage.

## 1. Introduction

Nowadays, many research fields are combined and used in various areas and applications. In the field of power electronics we are currently talking about new concepts such as real-time and hardware implementation, despite the fact that these notions were reserved for information sciences for a few years. In-fact, advancement in the numerical control methods of machines has led to complex and heavy algorithms concerning processing time. In parallel with these advancements, other advancements are also noticed in the digital systems field and especially in the field of reconfigurable circuits (FPGA: Field programmable Gate Array). These devices are generally used to realize the necessary degrees of parallelism and pipelining in order to accelerate the data processing in various algorithms and in order to realize the real time of various implementations.

In this paper, we present several hardware implementations of Sinusoidal Pulse Width Modulation (SPWM) Applied for Medium-Voltage Source Converter-Based Drives (MV-CSC). The purpose of this work is to build a library of Hardware IPs concerning the SPWM and to use these IPs according to the needs of various applications. To avoid details of HDL programming and to perform fast simulations, we use the new Xilinx System-Generator (XSG) tool for the implementation, the simulation and the synthesis of the proposed hardware implementations [1]. System-Generator is a new Xilinx-tool integrated into the Matlab-Simulink environment. It allows the auto-generation of HDL codes from a high-level specification while carding the possibility of using the simulation to. Using XSG, the results of the final simulation and synthesis are presented and commented.

The rest of this paper is organized as fellow: section 2 describes the proposed software and hardware implementations for the SPWM. In this section we present various simulation results using Matlab/Simulink and XSG. Section 3 shows harmonic spectrum results and synthesis results. Finally, we present the conclusions and future works in section 4.

## 2. Software and hardware implementations of the SPWM

In this section we propose two different implementations of the SPWM technique using the Matlab/Simulink and the XSG. Eventually we compare simulations results.

### 2.1. Simulation of the SPWM technique using Matlab/Simulink

In this section we simulate the three-phase SPWM used to control a two-level three-phase inverter connected to an RL load [2]. This technique is composed mainly by two chains: generation of a triangular signal and generation of three sinusoids displaced by 120 degrees from each other. In this technique we also use three comparators to compare the triangular signal to the three generated sinusoids. Figure 1 shows the SPWM schematic and a three phase inverter [3] performed under Matlab-Simulink with RL charge (Vdc=230v, R=10Ω and L=0.001H).

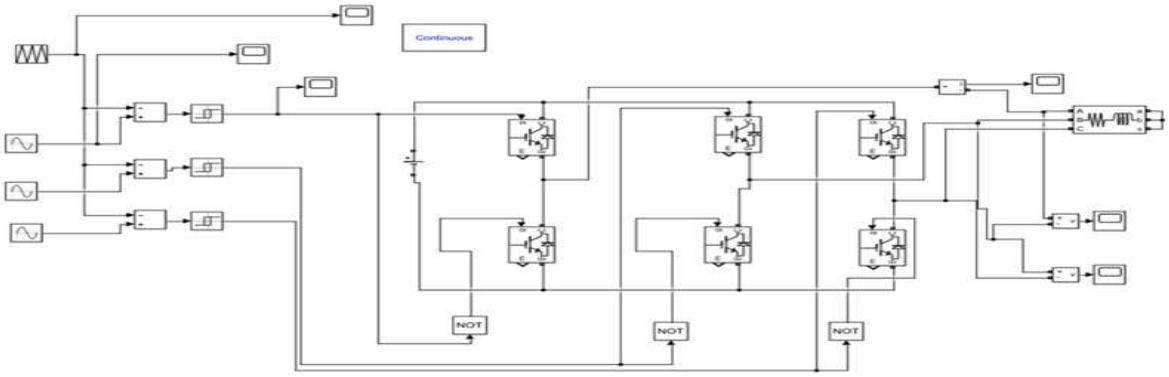
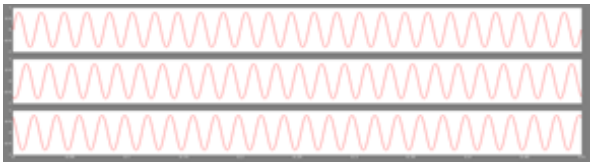
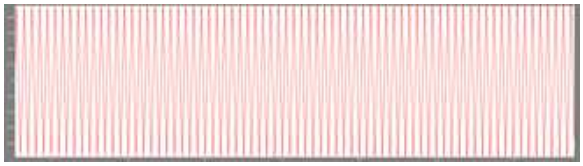



**Fig.1.** Sine-triangular PWM simulation schemes for three phase inverter

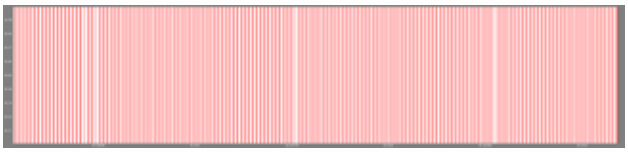
Figure 2 shows the simulation results at different stages of the SPWM. Figures 2.a, b and c show respectively the three generated sinusoids, the triangular signal and the control signal (SPWM). Figure 2.d shows the line voltage of the inverter output. Figure 2.e shows the phase voltage of the inverter output. Figure 2.f shows the phase current of the inverter output.



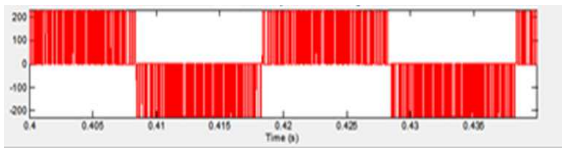
(a) The three sinusoids



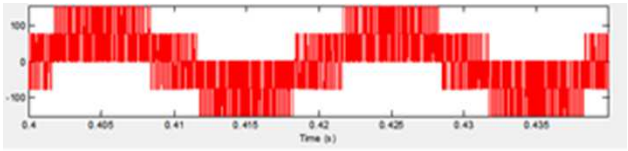
(b) The triangular signal



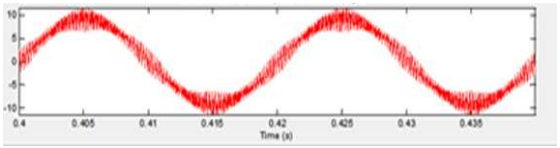
(c) The PWM control signal for a inverter arm.




d) Voltage composed of the inverter output.




e) The single voltage of the inverter output.




f) Phase current

**Fig.2.** The SPWM simulation results

## 2.2. Hardware implementations of SPWM using XSG

In this step, we generate the sine-triangular PWM signal using the Xilinx blockset. For hardware implementations, we use the two cards from Xilinx (XUPV5 and Zed-Board) respectively equipped with FPGA circuits of Virtex5-LX110T and Zynq-7000 type. FPGA cards are a good solution for implementing control laws, including sine-triangular PWM.

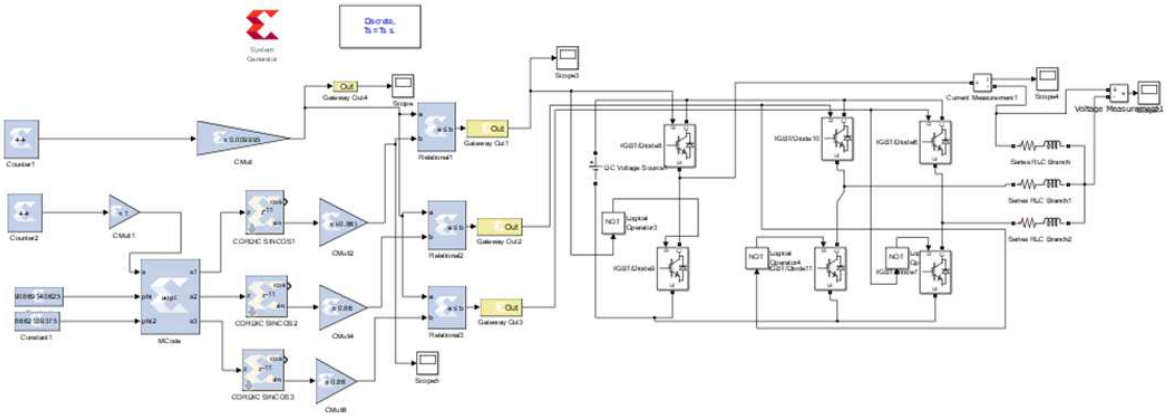


**Fig.3.** The proposed model for the SPWM using XSG

Figure 3 shows the proposed scheme for the PWM Sinus-Triangular command using the Xilinx System-Generator tool. The aim of this proposal is to carry out a co-simulation of the hardware implementations by taking advantage of the simulation tools offered by Matlab-Simulink. We can however move to a hardware implementation of these proposals on FPGA cards after a few steps of HDL conversion, allocation of inputs/outputs and finally the synthesis step. We can even use these implementations as hardware accelerators using the "in-the-loop" technique.

The SPWM command is composed by two chains for the generation of the two signals (Sinusoidal and triangular). These two chains provide the inputs of a comparator with a Boolean output. In this part of the present work, we only use Xilinx blocks [4] for the generation of these two signals.

### 2.2.1. Details of Xilinx blocks used

The 'System Generator' blog is the main block in the architecture modelled using Matlab-Simulink and XSG. In this module, we can manually configure the link between the hardware and the simulation parts. It allows specifying the FPGA device and the used language for the hardware implementation in order to generate the file to be implemented on FPGA targets using the Xilinx tools. We used a period of the Simulink system equal to 10e-08 (sec), which is equivalent to a frequency of 100MHz. This frequency is available at the input (AH15) on the Xilinx-XUPV5 card and on several other cards from.

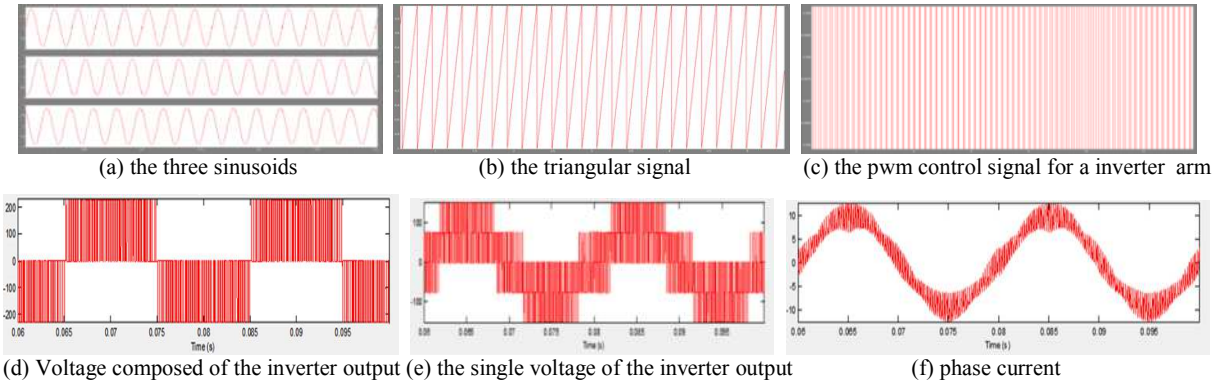
For the generation of the triangular signal, we use a first counter "Counter1: 8bits Xbits" with parameters (initial value = -100, explicit period Ts = $2^{-20}$). We also use a multiplier to ensure a real triangular signal varying between 0 and 1. The operating frequency (10KHZ) of the moduloX counter depends on the precision requested (in our case, we use a frequency of the order of $1/10^{-4}$). The operating frequency of the modulo1 counter is calculated according to the first frequency (F2 = F1 / 2X). To ensure a real triangular signal varying between 0 and 1, we use a multiplication coefficient equal to 1/100.

For the generation of the sinusoidal signal, we use the CORDIC block. Indeed, the CORDIC is an algorithm used for the generation of trigonometric functions. Xilinx offers several types of CORDIC blocks. We use the simple CORDIC block "CORDIC SINCOS" with a single input and two outputs (sine and cosine). Several parameters are necessary for the configuration of this block: the method used, pipeline or not, latency, etc. The input of this block is a signal varying from $+\pi$ to $-\pi$ provided by a 20bits counter (-1 / Ts / 100 until 1 / Ts / 100) combined with a gain (Cmult1) with constant value 1, The CORDIC block calculates the sine / cosine of a single value, which implies that the time axis at the input of this block must be ensured.

An MCODE function is used to ensure the 120° offset between the three sinusoidal signals, the operating frequencies must be chosen to synchronize the operation of the different blocks and to generate a sinusoidal signal close to reality. We also used a Xilinx "Relational" block to compare the signals. The output signal of the comparators are inverted for the generation of the 2 PWM control signals necessary for the control of an inverter with even Xilinx blocks for the management of dead time. The Gateway Out blocks are used for converting the output signals before they are displayed on the oscilloscope under Matlab / Simulink [5].

### 2.2.1. Simulation results

The following figures show the simulation results of the sine-triangular PWM signal of the Xilinx block-based model for simulation and hardware implementation on an FPGA circuit, Figures 4.a,b and c show respectively the three generated sinusoids, the triangular signal and the control signal (SPWM). Figure 4.d shows the line voltage of the inverter output, Figure 4.e shows the phase voltage of the inverter output. Figure 4.f shows the phase current of the inverter output.



(a) the three sinusoids (b) the triangular signal (c) the pwm control signal for a inverter arm

(d) Voltage composed of the inverter output (e) the single voltage of the inverter output (f) phase current

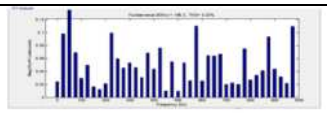
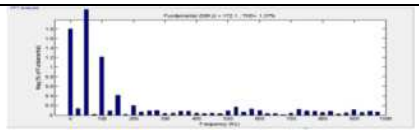
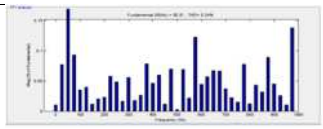
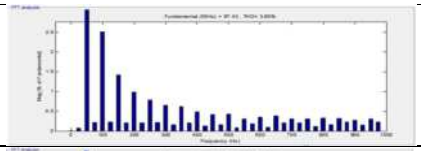
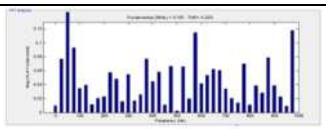
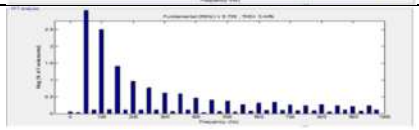
**Fig.4.** Implementation results of SPWM using XSG

## 3. Results and Discussion

### 3.1. Harmonic spectrum result

Table 1 shows simulation results on Matlab and implementation on Xilinx System generator for inverter output voltage and phase current, the results obtained on System Generator are better on the harmonic spectrum side.

**Table1.** Harmonic spectrum result

| | Matlab/simulink | | Xilinx system Generator | |
|---|---|---|---|---|
| **Parameter** | **Harmonic spectrum** | **THD %** | **Harmonic spectrum** | **THD %** |
| **Voltage composed** |  | 0.33 |  | 1.37 |
| **single voltage** |  | 0.34 |  | 3.6 |
| **phase current** |  | 0.32 |  | 3.44 |

### 3.2. Synthesis and Implementation Results:

System-Generator allows self-generation of HDL (VHDL or Verilog) codes from a high-level specification (Simulink model). It also allows the transition directly to the NGC level or to the generation of binary codes of FPGA circuit configuration; Table 2 shows Synthesis and Implementation Results.

**Table 2.** Synthesis and Implementation Results

| | Slices registers | BRAMs | Slices LUTs | MULTs/DSP48s |
|---|---|---|---|---|
| Used | 529 | 0 | 1859 | 0 |
| Available (LX110T) | 69120 | 148 | 69120 | 64 |
| Available (Zynk7000) | 106400 | 140 | 53200 | 64 |

## 4. Conclusion

The implementation of SPWM technique on Matlab/Simulink and System Generator allowed us to show the similarity of the results between the two systems for the generated PWM signal and the waveform side of the output and current voltages, the percentage THD is better for Matlab/Simulink on the contrary the elimination of harmonics at a limit of 1000Khz shows us the effectiveness of the FPGA. The use of the Resources Estimator tool of Xilinx system generator allowed us to obtain the results of synthesis and implementation.

## References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