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# Modeling and simulation of thermal behavior in field effect transistor systems

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**Abstract**

The field effect transistor is the backbone of semiconductor electronics today. Among the transistor devices used is the metal semiconductor field effect transistor (MESFET). This device has an important role in electronic circuits in terms of resistance to the passing electric current and controlling the intensity of this current. As the size of the device decreases on the nanoscale, the heat generated affects the efficiency of the device. In this work, we studied the heat transfer inside the MESFET device based on gallium arsenide using the lattice Boltzmann method (LBM) with the effect of the specularity parameter which affects the thermal conductivity of the device and a change in the device substrate where used silicon, silicon oxide and gallium arsenide . The results showed that the device based on silicon substrate is less hot than the device based on silicon oxide and gallium arsenide, and that increasing the specularity coefficient has a positive effect on reducing the temperature of electronic devices.
***Keywords*** **:** MESFET; heat transfer ; Lattice Boltzmann method ; Gallium arsenide; Substrate.

**الملخص**

ترانزستور ذو التأثير الحقلي هو العمود الفقري لإلكترونيات أشباه الموصلات اليوم، من بين اجهزة الترانزستور المستعملة هو ترانزستورمعدني شبه موصل ذو التأثير الحقلي ميسفت (MESFET) حيث ان هذا الجهاز له دور مهم في الدوائر الالكترونية من حيث المقاومة التيار الكهربائي المار والتحكم في شدة هذا التيار .ومع تناقص حجم الجهاز على مقياس النانو، فإن الحرارة المتولدة تؤثر على كفاءة الجهاز .في هذا العمل قمنا بدراسة الانتقال الحراري داخل جهاز ميسفت المعتمدة على زرنيخيد الغاليوم مع تأثير معامل الانعكاسية الذي يؤثر على التوصيل الحراري للجهاز وتغيير في ركيزة الجهاز حيث تم استعمال سليكون واوكسيد سليلكون و زرنيخيد الغاليوم، وذلك باستخدام طريقة شبكة بولتزمان .أظهرت النتائج أن الجهاز المعتمد على ركيزة السيليكون أقل حرارة من الجهاز المعتمد على واوكسيد سليلكون و زرنيخيد الغاليوم ، كما أن زيادة معامل الانعكاسية له تأثير إيجابي على خفض درجة حرارة الأجهزة الإلكترونية.

**الكلمات المفتاحية :** ميسفت؛ انتتقال الحرارة ؛ طريقة شبكة بولتزمان ؛ زرنيخيد الغاليوم ؛ الركيزة

**Résumé :**

Le transistor à effet de champ constitue aujourd'hui l'épine dorsale de l'électronique à semi-conducteurs. Parmi les dispositifs à transistors utilisés le transistor à effet de champ métal-semiconducteur (MESFET). Ce dispositif a un rôle important dans les circuits électroniques en termes de résistance au courant électrique qui passe et de contrôle de l'intensité de ce courant. À mesure que la taille du dispositif diminue à l'échelle nanométrique, la chaleur générée affecte l'efficacité du dispositif. Dans ce travail, nous avons étudié la transfert de chaleur à l'intérieur du dispositif MESFET à base d'arséniure de gallium en utilisant la méthode de Boltzmann sur réseau (LBM) avec l'effet du paramètre de spécularité qui affecte la conductivité thermique du dispositif et un changement dans le substrat du dispositif où il est utilisé. Silicium, oxyde de silicium et arséniure de gallium. Les résultats ont montré que le dispositif à base de substrat de silicium est moins chaud que le dispositif à base d'oxyde de silicium et d'arséniure de gallium, et que l'augmentation du coefficient de spécularité a un effet positif sur la réduction de la température des dispositifs électroniques.
**Mots clés** : MESFET ; Transfert de chaleur ; Méthode de Boltzmann sur réseau ; Arséniure de gallium ; Substrat.

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First, we thank **ALLAH**, our creator for giving us the strength to do this work.

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# Dedication

***To our parents,***

***To our family,***

***To our friends.***

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## Nomenclature

| | | | |
|---|---|---|---|
| $c$ | lattice velocity, m $s^{-1}$ | $x, y$ | Directions, m |
| $L_c$ | Channel length, m | | |
| $C$ | Volumetric heat capacity, J $m^{-3}$ $K^{-1}$ | $\theta_D$ | Debye temperature, K |
| $j$ | Phonon distribution function | $\Lambda$ | Phonon mean free path, m |
| $\hbar$ | Planck constant divided by 2π, J s | $\eta$ | Number density of oscillators, $m^{-3}$ |
| $k$ | Thermal conductivity, W $m^{-1}$ $K^{-1}$ | $\tau$ | Phonon relaxation time, s |
| $Kn$ | Knudsen number, $\Lambda/L_c$ | $\omega$ | Phonon frequency, $s^{-1}$ |
| $k_B$ | Boltzmann constant, J $K^{-1}$ | | |
| $a$ | Adjustable coefficient | $i$ | Discrete direction |
| $q_v$ | Heat generation rate per unit volume, W $m^{-3}$ | | |
| $u$ | Phonon energy density, J $m^{-3}$ | | |
| $v$ | Phonon group velocity, m $s^{-1}$ | $eq$ | Equilibrium |
| $t$ | Time, s | * | Dimensionless |
| $T$ | Temperature, K | | |
| FET | Field Effect Transistor | Si | Silicon |
| MOSFET | Metal oxide semiconductor field effect transistor | GaAs | Gallium arsenide |
| JFET | Junction field effect transistor | Ge | Germanium |
| MESFET | Metal semiconductor field effect transistor | GaN | Gallium nitride |
| HEMT | High electron mobility transistor | BTE | Boltzmann Transport Equation |
| FeFET | Ferroelectric field effect transistor | LBM | Lattice Boltzmann method |
| ETC | Effective thermal conductivity | MES | Metal semiconductor |

# General introduction

With the developments of electronic devices from the era of industry up to the era of technology, they have evolved significantly and everything has emerged from them to make our lives easier and simpler. Electronic devices are machines that were developed to serve humans to make their environment and life easier in all fields. The semiconductor transistor is considered one of the basic components in every electronic device so that it controls. In the flow of electrical current for information processing and system control. The current trend towards nanoscale electronics has led to enormous levels of integration in recent years, with the assembly of hundreds of millions of semiconductors on an area not exceeding a few square centimeters for integrated circuits [1, 2]. There are many type of field-effect transistor (FET) that are used in many different types of electronic circuits such as JFET , MESFET and MOSFET…etc. These devices have an important role in controlling the electrical current passing through it [1, 2].

The average free path of the phonon on which transistors are based is around the same or less than the feature size of electronic devices found in today's integrated circuits. This shrinking had an impact on transistors, causing the electronic device's channel area to shrink below the phonon, or free path. Examining the heat transmission within the nanoelectronic device terminal is crucial for demonstrating the thermal stability and effectiveness of integrated circuits made up of transistors. The Joule effect can produce heat in very small semiconductor devices that prevents the device's operational power from being lowered below a particular point. Additionally, electronic device switching times approach phonon relaxation [3, 4]. Due to the heat carriers' finite relaxation period, it is well known that heat transfer at the nanoscale may differ significantly from Fourier's law. The mechanism of heat transfer in structures is investigated using the Boltzmann transport equation (BTE) and the Monte Carlo solution method. The meso-scale method generates statistical information (particle distribution function) in a subcontinuous medium because of particle movement [5, 6].

Macroscopic equations were relied upon to study heat transfer in nanometer-sized objects, but these equations require additional variables or components that must be added to the equation in order to improve its ability to study thermal diffusion inside nanoscale objects. However, it was suggested in this work that thermal behavior inside a MESFET be studied using the Boltzmann

lattice method, which is based on the Boltzmann equation with different three substrates (Si ,GaAs, $SiO_2$) and the effect of the reflectivity coefficient.

The following is the work's organization: The first chapter provides an overview of transistor electronic device technology, including topics such as the device's multiple forms, operation, developmental stages, size, and several prior research projects. The Lattice Boltzmann approach was selected in chapter two for a number of reasons, including its great computing efficiency, ease of programming, and mathematical and physical modeling. The boundary conditions can be implemented in this geometry can be achieved using this method. The simulated results using the LBM model that was used to study heat behavior in MESFET nanadevice are shown in chapter three .

# Chapter I: State of the art technology: Field Effect Transistor (FET)

# I. Introduction

We shall examine field effect transistors (FETs) in this chapter. The majority of these live devices are rack devices, which are quite simple and adaptable to build. These days, FETs may be made from a large variety of materials, including Si, SiGe, GaAs, InGaAs, GaN, and SiC.

The FET operates on a very basic premise. Electrons (or holes) go from the source to the drain via an active channel in the device. Ohmic connections make up the source and drain contacts. A voltage supplied to the gate modifies the conductivity of the channel. As a result, the charge density traveling across the channel is modulated. To ensure that no current enters the gate, it is crucial to isolate it from the channel. There are several methods for achieving gate isolation, which result in a multitude of devices. An oxide separates the MOSFET's gate from the channel. The silicon devices are built on this foundation.

The gate of a metal-semiconductor FET, or MESFET, forms a Schottky barrier with the semiconductor, and within the practical gate voltage range, the gate current is low. A p-n junction is employed in reverse bias in junction FETs, or JFETs, to isolate the gate. A high bandgap semiconductor is used in heterojunction field effect transistors (HFETs) or modulation doped FETs (MODFETs) to separate the gate from the active channel.

## I.2. History and development of FET

The field-effect transistor (FET) was first patented by Julius Edgar Lilienfeld in 1925[7] and Oskar Heil in 1934, but it was not built into a practical semiconducting device. John Bardeen and Walter Houser Brattain later observed and explained the transistor effect while working under William Shockley at Bell Labs in 1947. They attempted to build a working FET by modulating the conductivity of a semiconductor but were unsuccessful due to problems with surface states, dangling bonds, and germanium and copper compound materials[8, 9].

The first FET device to be successfully built was the junction field-effect transistor (JFET)[8], which was first patented by Heinrich Welker in 1945. The static induction transistor (SIT) was invented by Japanese engineers Jun-ichi Nishizawa and Y. Watanabe in 1950. George C. Dacey and Ian M. Ross built a working practical JFET in 1953[10]. However, the JFET still had issues affecting junction transistors in general, making them difficult to manufacture on a mass-production basis.

The foundations of MESFET technology were laid down by the work of William Shockley, John Bardeen, and Walter Brattain. Bardeen's surface state hypothesis marked the birth of surface physics and led to the invention of an insulated-gate FET (IGFET) with an inversion layer in 1948. This concept forms the basis of CMOS technology today[11].

In 1955, Carl Frosch and Lincoln Derrick discovered the passivating effect of oxidation on the semiconductor surface and developed oxide diffusion masking, which would later be used in the fabrication of MOSFET devices[12, 13].

## I.3. Types of FET

One may create a p-type or an n-type semiconductor by doping the channel of a FET. In enhancement mode FETs, the drain and source may be doped with a different type than the channel; in depletion mode FETs, the drain and source may be doped with a different type than the channel. Another characteristic that sets field-effect transistors apart is the way the channel and gate are insulated. Among the FET types are:

### I.3.1. The Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET):

It is a form of field-effect transistor (FET), which is generally made by carefully oxidizing silicon. It features an insulated gate, the voltage of which controls the device's conductivity. Electronic signals can be amplified or switched using this property of conductivity changing with applied voltage. MOSFET and metal-insulator-semiconductor field-effect transistor (MISFET) are nearly interchangeable terms. The insulated-gate field-effect transistor (IGFET) is another similar replacement.[14].

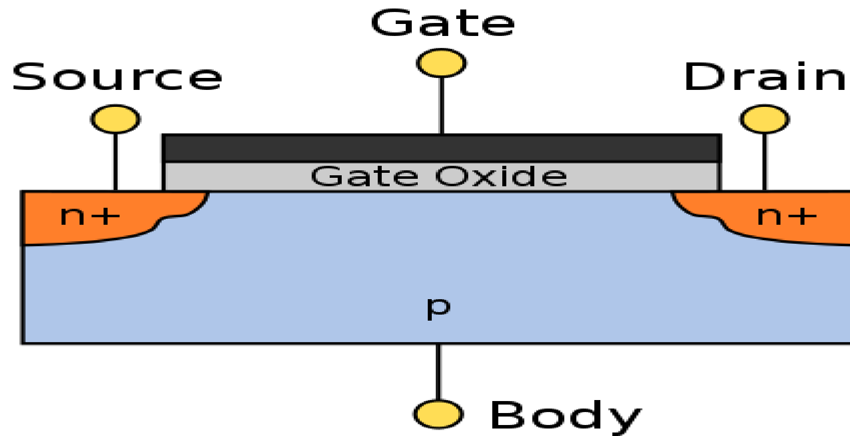



**Fig I.1:** Cross section of a MOSFET [15].

### I.3.2. The junction field-effect transistor (JFET):

It is a simple type of field-effect transistor that can be used as switches, resistors, or amplifiers. JFETs are voltage-controlled and do not require a biasing current[16]. Electric charge flows through a semiconducting channel between source and drain terminals. A reverse bias voltage pins the channel, preventing the electric current from flowing. JFETs are usually conducting when there is zero voltage between them. If a potential difference of the proper polarity is applied, the JFET becomes more resistive to current flow, reducing current flow. They are also known as depletion-mode devices, relying on a closed depletion region. JFETs can have an n-type or p-type channel, with a large input impedance reducing current draw from circuits used as input to the gate.

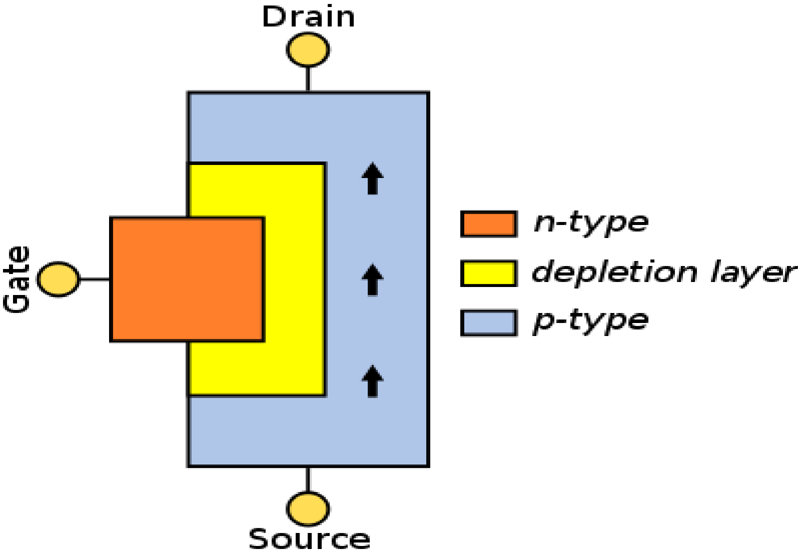



**Fig I.2:** An illustration of a JFET (junction-gate field-effect transistor)[17].

### I.3.3. (MESFET):

Similar to a JFET, a MESFET (metal-semiconductor field-effect transistor) is a semiconductor field-effect transistor device that uses a Schottky (metal-semiconductor) junction for a gate rather than a p–n junction.

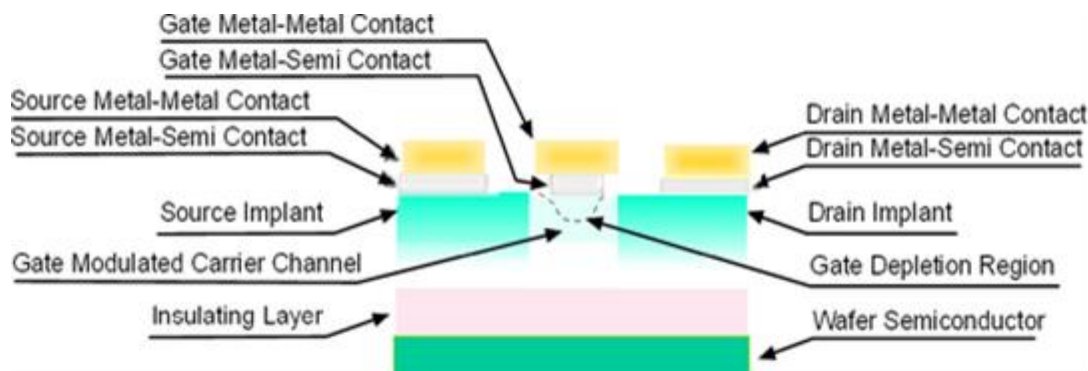



**Fig I.3:** MESFET schematic[18].

### I.3.4. A high-electron-mobility transistor (HEMT):

is a field-effect transistor with a junction between two materials with different band gaps. Common materials include GaAs with AlGaAs. Indium-containing devices show better high-frequency performance, while gallium nitride HEMTs have high-power performance. HEMTs are used in integrated circuits as digital on-off switches and amplifiers for large currents. They operate at higher frequencies, making them popular in high-frequency products like cell phones, satellite receivers, and radar equipment.

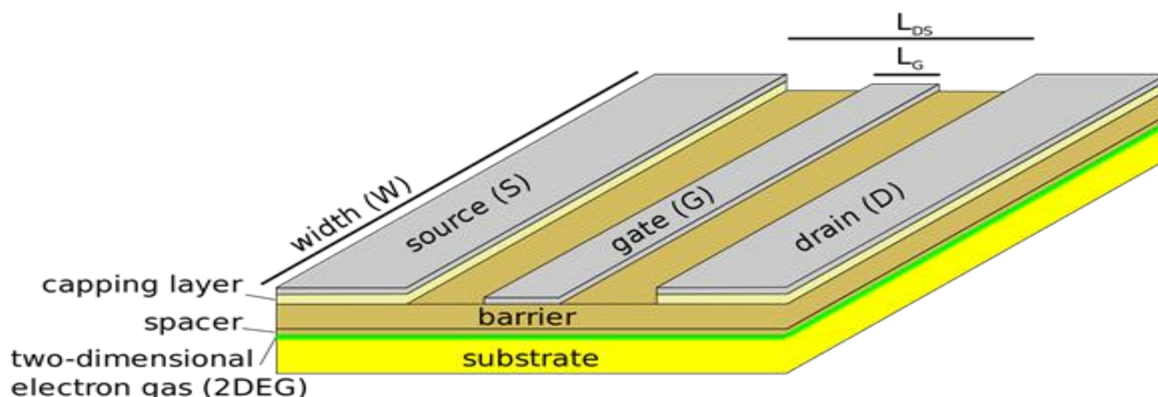



**Fig I.4:** Cross section of a GaAs/AlGaAs/InGaAs pHEMT[19].

### I.3.5. FINFET:

is a multigate device, a MOSFET (metal-oxide-semiconductor field-effect transistor) constructed on a substrate in which the gate is positioned around the channel, creating a double or even multiple gate structure, or on two, three, or four of the channel's sides. The reason behind the generic term "FinFETs" for these devices is because the silicon surface has fins formed by the source/drain area. Compared to planar CMOS (complementary metal-oxide-semiconductor) technology, FinFET devices have substantially quicker switching times and greater current densities[16].

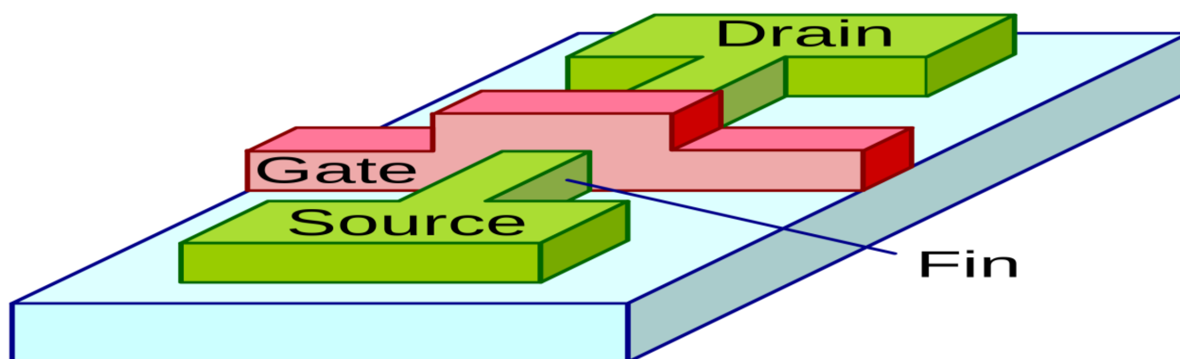



**Fig I.5:** A FinFET with two gates[20] .

### I.3.6. ferroelectric field-effect transistor (Fe FET):

A ferroelectric substance is positioned between the gate electrode and the source-drain conduction portion of the device (the channel) in a ferroelectric field-effect transistor, or Fe FET. In the absence of any electrical bias, this kind of device maintains the transistor's state (on or off) due to permanent electrical field polarization in the ferroelectric.

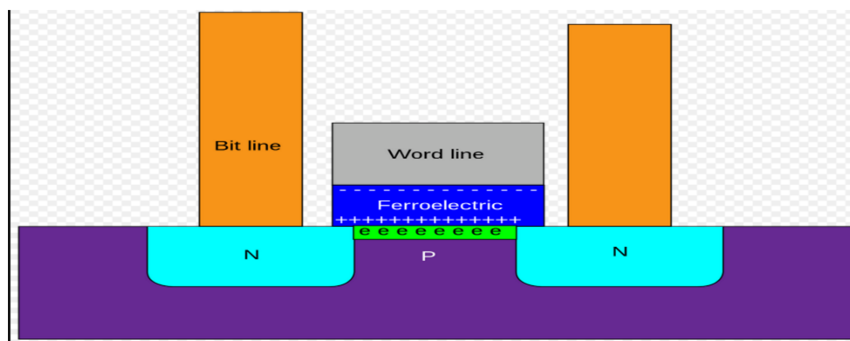



**Fig I.6:** Structure of a 1 Transistor FeRAM cell[11]

## I.4. FET structure

FETs fall into one of two categories: majority-charge-carrier devices, in which the bulk of the current is carried by the majority carriers, or minority-charge-carrier devices, in which the current is mostly caused by a flow of minority carriers.Through the active channel of the device, charge carriers such as electrons or holes travel from the source to the drain. The source and drain terminal conductors are connected to the semiconductor via ohmic connections. The conductivity of the channel is determined by the voltage across the gate and source terminals [21].

**There are three terminals on the FET:[15]**

**Point of entry (S) :** through which the carriers enter the channel. $I_S$ is typically used to identify the current entering the channel at S

**drain (D):** $I_S$ represents the point at which carriers quit the channel. Current enters the channel at S. $I_D$ is commonly used to detect current exiting the channel at D.

**Gate (G):** which controls the conductivity of the channel, is the drain-to-source voltage ($V_{DS}$). Voltage applied to G allows control over $I_D$.

More about terminals:

Like BJTs, FETs feature source, drain, and gate terminals. Additionally, they have a fourth terminal that biases the transistor and is referred to as the body, base, bulk, or substrate. The length L, or the gap between source and drain, represents the gate's size. The transistor's width is its extension perpendicular to the cross section. Usually, the breadth is more than the length of the gate. The top frequency limit is set at 1 µm for gate lengths and at 30 GHz for 0.2 µm gate lengths.

The term "terminals" in a semiconductor refers to its operational components, such as the physical gates that open and close to permit or prohibit electron passage by establishing or obstructing a channel between the source and the drain. The gate, source, and drain are located in the middle of the semiconductor, which is referred to as the body. Depending on the kind of FET, the body terminal is often linked to either the highest or lowest voltage in the circuit. Transmission gates and cascode circuits are two applications for FETs that do not require connections between the body and source terminal.

The great majority of FETs have electrical symmetry, in contrast to BJTs. Thus, in real circuits, the source and drain terminals may be switched around without affecting the circuit's functionality

or operating characteristics. When FETs seem to be linked "backwards" in schematic designs and circuits, this might be perplexing since the FET's physical orientation was chosen for other reasons, such printed circuit layout constraints.

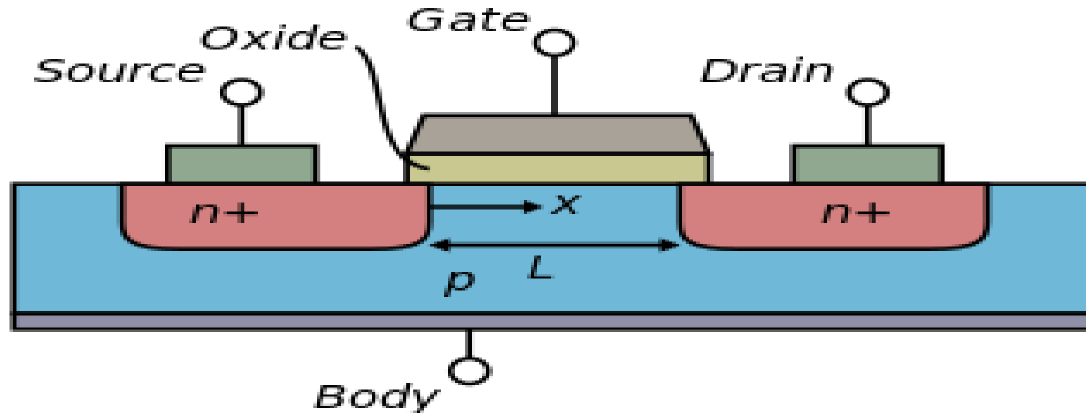



**Fig I.7:** Sectional view of an n-type MOSFET [22]

## I.5. How the FET works and how to control the current:

**Effect of gate voltage on current:** By adjusting the dimensions and configuration of a "conductive channel" formed and impacted by voltage (or lack thereof) placed across the gate and source terminals, the FET regulates the flow of electrons (or electron holes) from the source to the drain. (For the sake of simplicity, let's suppose that the source and the body are related.) The "stream" that electrons travel in as they go from the source to the drain is this conducting channel.

**n-channel FET:**A negative gate-to-source voltage in an n-channel "depletion-mode" device causes a depletion area to widen and encroach on the channel from the sides, narrowing the channel. The FET is essentially switched off like a switch if the active zone widens to completely close the channel (see right picture, when there is very little current). This happens when the resistance of the channel increases from source to drain. The voltage at which this happens is referred to as the "pinch-off voltage" and is known as "pinch-off". In contrast, a positive gate-to-source voltage widens the channel and facilitates easy electron passage (see right figure, in the case of a conduction channel with a high current).

An n-channel "enhancement-mode" device needs a positive gate-to-source voltage because a transistor lacks a conductive channel by design. The positive voltage attracts free-moving electrons in the body to the gate, forming a conductive channel. This occurs at a voltage known as the FET's threshold voltage. To counterbalance the dopant ions supplied to the FET's body, enough electrons must be pulled to the gate before this can occur. This results in the creation of the depletion region, an area devoid of mobile carriers. By raising the gate-to-source voltage even further—a process known as inversion—more electrons will be drawn to the gate and an active channel from source to drain can be formed.

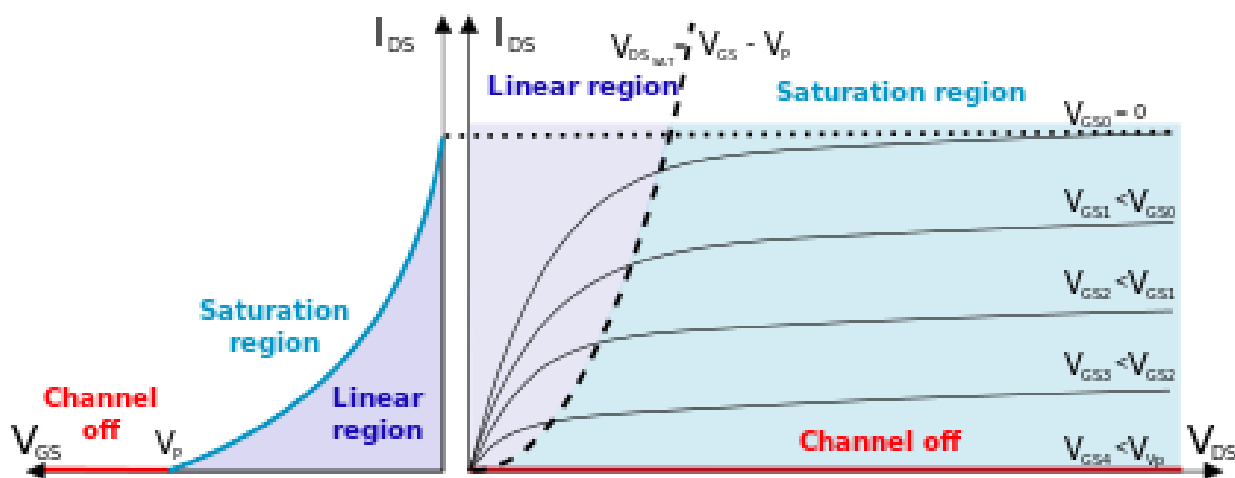



**Fig I.8:** Properties and graphs of an N-channel JFET transistor[23]

**p-channel FET**: The depletion layer of a p-channel "depletion-mode" device is extended by applying a positive voltage from the gate to the body. This voltage drives electrons to the gate-insulator/semiconductor interface, exposing a carrier-free region of stationary positively charged acceptor ions.

On the other hand, negative voltage is required to create a conduction channel in a p-channel "enhancement-mode" device as there isn't a conductive area there.

**Effect of drain-to-source voltage on channel:** The drain current is proportional to the drain voltage (referenced to source voltage), therefore altering the gate voltage will alter the channel resistance for both enhancement- and depletion-mode devices at drain-to-source voltages far lower

than gate-to-source voltages. The FET operates in what is known as an ohmic mode, or linear mode, when it performs like a variable resistor[24, 25]

A gradient of voltage potential caused by increased drain-to-source voltage causes a notable asymmetrical shift in channel geometry. When the voltage climbs further, the pinch-off point shifts from the drain towards the source, causing the inversion area to become "pinched-off" close to the drain end. Utilized for amplification, the FET is in saturation mode, also known as active mode. Even in cases when drain current and drain voltage are not linear, the intermediate zone may be regarded as a component of the ohmic or linear region.[26, 27]

In saturation mode, carriers continue to flow, but the source and drain are no longer connected by the conductive channel formed by the gate-to-source voltage. A depletion zone that surrounds the conductive channel, drain, and source regions is where an electron can leave the p-type body if it is drawn to the drain by the drain-to-source voltage. Its silicon-like resistance causes the drain-to-source current to remain virtually constant when the drain-to-source voltage increases. In saturation mode, the FET acts as a voltage amplifier and constant-current source, and the gate-to-source voltage regulates the constant current level across the channel.

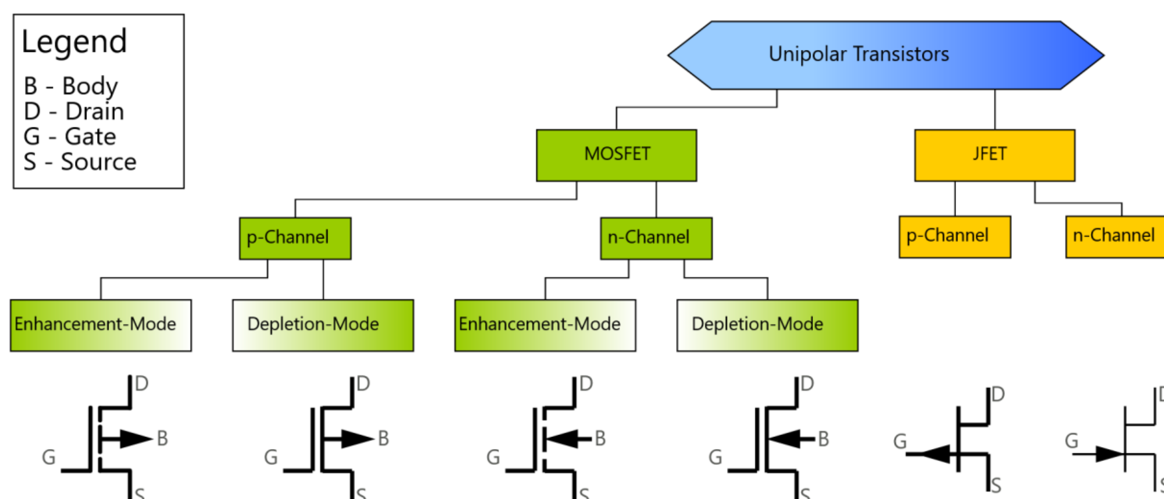



**Fig I.9:** standard symbol types for FETs[20]

## I.6. Applications of FETs:

FETs have special properties that make them useful in a variety of applications. The following are a few of the main applications:

**Amplifiers:** FETs are frequently utilized in amplifier circuits because of their high input impedance and low power consumption.

**Electronic switches:** FETs, particularly MOSFETs, are widely employed as electronic switches in digital circuits.

**Buffers:** Because of its high input impedance and low output impedance, FETs are utilized in voltage buffer applications.

**Charge Storage:** FETs are helpful in dynamic random-access memory (DRAM) cells because of their capacitor structure, which enables them to store charge.

## I.7. Semicoductor materials :

- **Si material:**The electronics and solar photovoltaic industries employ high purity polycrystalline silicon, sometimes known as multicrystalline silicon, polysilicon, poly-Si, or mc-Si, as a raw material[28].
- **GaAs material**: The crystal structure of gallium arsenide (GaAs), a direct band gap semiconductor, is zinc alloy. Microwave integrated circuits, monolithic microwave integrated circuits, infrared light-emitting diodes, laser diodes, and solar cells are components made of gallium arsenide. and windows with optics[29].
- **Ge material:** The chemical element germanium has the atomic number 32 and the symbol Ge. It looks like silicon and is glossy, hard-brittle, and grayish-white in color. It is a metalloid in the carbon group that shares chemical similarities with tin and silicon, two of its group neighbors. Similar to silicon, germanium naturally interacts with oxygen to generate complexes[30].
- **GaN material:** A sensitive semiconductor, gallium nitride finds use in radiation-hardened military and space applications as well as photovoltaic cells that power satellites. Compared to GaAs transistors, it can work at higher temperatures and voltages, which makes it effective for power

amplification in the microwave range[31]. In the terahertz region, GaN exhibits great potential and may be found in alloys used in photodiodes, some JFETs, and MODFET (HEMT) devices[31].

| | Ge | Si | GaAS | 3H-SIC | 4H-SIC | 6H-SIC | GaN | Diamamnt |
|---|---|---|---|---|---|---|---|---|
| Bande interdite $E_c$ (eV) | 0.66 | 1.1 | 1.4 | 2.2 | 3.26 | 3 | 3.39 | 5.45 |
| Champ.claqu.$E_c$ (MV/cm) | 0.1 | 0.3 | 0.4 | 1.2 | 2 | 2.4 | 3.3 | 5.6 |
| Constant.dielectrique $\varepsilon$ r | 16 | 11.8 | 12.8 | 9.6 | 10 | 9.7 | 9 | 5.5 |
| Mobil.elec $\mu_n$ ($cm^2.V^{-1}.s^{1-}$) | 3900 | 1350 | 8500 | 900 | 720 | 370 | 900 | 1900 |
| Mobil.elec $\mu_p$ ($cm^2.V^{-1}.s^{1-}$) | 1900 | 420 | 320 | 40 | 115 | 90 | 30 | 1600 |
| Vites.sat.ele $V_{sat}$($10^7 cm.s^{-1}$) | 0.5 | 1 | 2 | 2 | 2 | 2 | 2.5 | 2.7 |
| Cond.therm $\lambda$ ($W.K^{-1}.cm^{-1}$) | 0.6 | 1.5 | 0.5 | 4.5 | 4.5 | 4.5 | 1.3 | 20 |

**Table I.1:** Lists some of the primary polytypes of SiC's physical characteristics and compares them to those of Ge, Si, GaAs, GaN, and diamond[32].

## I.8. Advantages of FET:

Control and flow are kept very apart in field-effect transistors due to their high gate-to-drain current resistance (of at least 100 MΩ). Since base current noise increases with shaping time, a FET typically produces less noise than a bipolar junction transistor (BJT), which is employed in noise-sensitive electronics such as tuners and low-noise amplifiers for VHF and satellite receivers[clarification needed]. With 0% drain current, it exhibits no offset voltage, making it an excellent signal chopper. It generally has better thermal stability than a BJT [15]

FETs are controlled by gate charge, in contrast to bipolar junction transistors or non-latching relays in some states, which would require additional power consumption after the gate is closed or open. This allows for extremely low power switching, allowing circuits to be more condensed because it requires less heat dissipation than other types of switches.

## I.9. Disadvantages of FET:

In comparison to the bipolar junction transistor, the field effect transistor has a very small bandwidth product. Because MOSFETs are highly susceptible to overvoltages, installation requires extra care. The MOSFET is susceptible to electrostatic discharge or variations in threshold voltage during handling due to the thin insulating layer that exists between the gate and the channel. Once the gadget is put in a circuit that has been appropriately built, this normally does not become an issue [13]

Often, FETs have very low "on" resistance and a huge "off" resistance. Nevertheless, due to their high average resistance, FETs can waste a significant amount of power when switching. In order to maximize efficiency, quick switching can therefore be essential. However, quick switching may also cause transients that excite stray inductances and generate high voltages that may couple to the gate and cause unexpected switching. Because of this, designing FET circuits may require careful consideration and may require balancing power dissipation and switching speed. Since there is a trade-off between voltage rating and "on" resistance, higher voltage FETs have relatively greater "on" resistance and hence conduction losses [14]

## I.10. Conclusion

Field-Effect Transistors, or FETs, are crucial parts of the electronics industry, to sum up. Their unique characteristics, which range from high input impedance to low power consumption and voltage control, make them invaluable in a variety of applications, from amplification to digital switching. Engineers can utilize the distinct advantages provided by the two main types of FETs: MESFETs and JFETs, depending on the requirements of the circuit. It is quite unlikely that the use of FETs in electrical design will become less common as technology develops.

# Chapter II: Lattice Boltzmann Methodology

## II.1 Introduction

The foundation of this approach is the Boltzmann equation, which was derived from Ludwig Eduard Boltzmann's Kinetic theory (Figure 2.1). Boltzmann was an Austrian physicist whose most notable contribution was the development of statistical mechanics, which describes and forecasts how to obtain the macroscopic properties of matter, such as density, viscosity, thermal conductivity, and diffusion coefficient, from the microscopic properties. A distribution function represents the property of the particle collection[33].

**Figure II.1: Ludwig Eduard Boltzmann (1844–1906)[34]**

For the past 200 years, solid modeling and transport phenomena have been extensively researched. There have been three primary methods (scales) used: macroscopic, mesoscopic, and microscopic theories. They both lead to the same set of macroscopic governing equations for the same system, although having distinct initial locations[35].

The system is evaluated at the macroscopic scale (continuum method), which ignores the behavior of individual molecules in favor of identifying the phenomenological qualities like pressure, velocity, and temperature.

The medium may be thought of as being composed of tiny particles at the opposite extreme, the microscopic size, and these particles smash with one another. In order to conserve the intended macroscopic values, it is based on discrete microscopic models such as Hamilton's equation and the ordinary differential equation of Newton's second law.

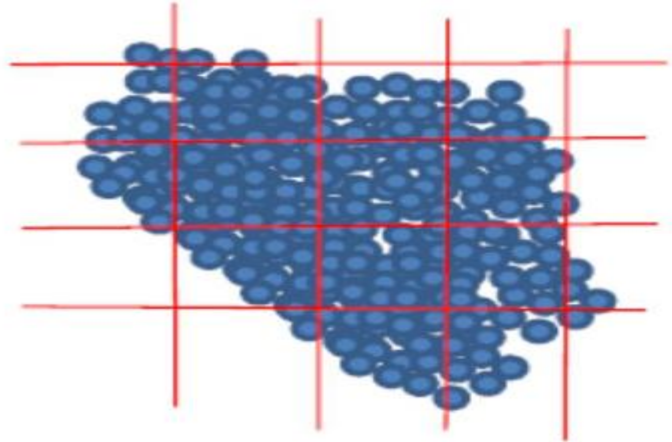
Boltzmann's primary goal is to close the gap between the micro and macro approaches by focusing on the behavior of a group of particles rather than the behavior of a single particle. This technique is known as mesoscopic scale, and Figure 2.2 illustrates the various approaches that are applied in the simulation of various types of problems.

The LB method has many appealing advantages over traditional computational solid dynamics methods, including easy implementation, natural parallelism, the capacity to handle complex geometry, the ease of handling solid-to-solid or solid-to-wall interactions, and boundary conditions like those in porous media[36, 37].

**Macroscopic scale** (Continuum approach)

$$Q = -\frac{\lambda dT}{dx}$$

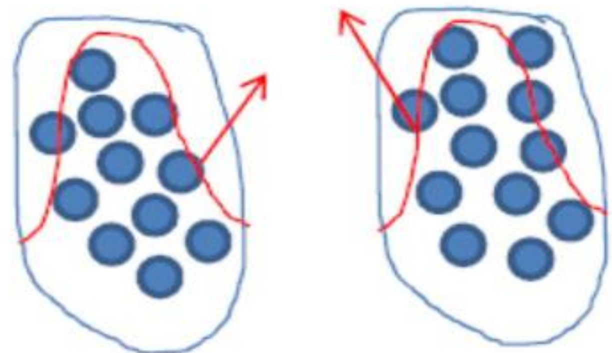
Fourier law equation



**Mesoscopic scale** (discrete approach)

Lattice Boltzmann method

Boltzmann equation



**Microscopic scale** (discrete approach)

Molecular Dynamics

Hamilton’s equation, Newton’s second

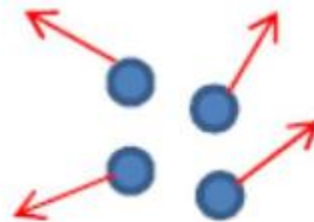


**Figure II.2:** different scales of simulation and modeling[38]

## II.2 Theory

Ludwig Eduard Boltzmann's Kinetic theory became the basis for the development of the Boltzmann Transport Equation (BTE). Boltzmann was an Austrian physicist whose theory formulation made a key addition to the science of statistical mechanics. This formula accounts for the motion of molecules and describes their behavior statistically as a function of space, velocity, and time.

## II.3 Phonon mechanism scattering process

The quantum mechanical term for a basic vibrational motion, such as the oscillation of an atom or molecule on a lattice, is a phonon. Many of the physical characteristics of materials, including thermal conductivity, are significantly influenced by phonons. Certain phonon characteristics are altered by the scattering processes they go through, depending on the kind of scattering process. Typical scattering mechanisms that a phonon experiences include[39]:

• Impurity scattering: This is mostly caused by crystal flaws, faults in the structure of the crystal, and impurities in the crystal.

• Phonon-phonon scattering: This type of scattering happens when two phonons collide as they move over a domain.

The phenomenon known as phonon-electron scattering occurs when an electron and a phonon collide.

• Interface scattering: When a foreign substance is introduced as an interface into a host material, it causes scattering events.

• Border scattering: This occurs when a phonon comes into contact with a domain border. The significance of these scatterings increases during the ballistic phase of phonon transport because of the small domain size and frequent encounters of the phonons with barriers.

## II.4 Phonon Boltzmann transport equation

Thermal energy in semiconductor materials mostly originates from phonons quanta of lattice vibrations. The thermal properties of semiconductor materials are determined by the ways in which phonons travel, clash, and interact with other carriers. This work uses the BTE, which accounts for phonon scattering, to investigate heat transfer in nano-transistors. To take into consideration the impact of heat transfer in the nanoscale devices, the transient Boltzmann transport equation for phonons is given by [40, 41]:

$$\frac{\partial j}{\partial t} + v.\nabla j = \frac{j^{eq} - j}{\tau} \qquad \text{(II.1)}$$

Here,j, $j^{eq}$, v, and τ stand for the phonon group velocity, equilibrium distribution function, phonon distribution function, and single relaxation time corresponding to resistive phonon collisions provided by[18, 42]:

$$\tau = \frac{3 \times k}{C \times v^2} = \frac{\Lambda}{v} \qquad \text{(II.2)}$$

Where thermal conductivity, mean free path, and volumetric heat capacity are represented by the letters k, Λ, and C, respectively. The following is the equilibrium distribution function for phonons as represented by the Bose-Einstein model[44 ‹43]:

$$j^{eq} = \frac{1}{e^{(\hbar\omega / k_B T)} - 1} \qquad \text{(II.3)}$$

The decreased Planck's and Boltzmann constants, denoted by ħ and $k_B$, respectively, in the equation above are represented by ω and T, which stand for the phonon frequency and absolute temperature, respectively. Eq. is used to determine the heat flux (II.4):

$$q = \sum_p \int v j \hbar \omega_p D_p(\omega) d\omega \qquad \text{(II.4)}$$

where the symbols p and $D_p$ stand for the phonon state density function and phonon polarization, respectively.

To make things easier, we may cast Eq. (II.1) into the phonon energy density BTE in the following way[34, 45]:

$$\frac{\partial e}{\partial t} + v.\nabla e = -\frac{e - e^{eq}}{\tau} + q_v \quad \text{(II.5)}$$

The quantum mechanical equation for phonons is another name for this formula, in which $q_v$ stands for volumetric heat generation.

A different definition of temperature is put forth, based on the assumption that the phonon energy at a particular temperature is equal to the total phonon energy in a given lattice point. In this way, the Debye model links the temperature and phonon energy[43, 46, 47]:

$$e(T) = \left( \frac{9\eta k_B}{\theta_D^3} \int_0^{\theta_D/T} \frac{z^3}{e^z - 1} dz \right) T^4 \quad \text{(II.6)}$$

Here, the Debye temperature, oscillator number density, and dimensionless variable are represented by the symbols $\theta_D$, $\eta$, and z, respectively.

## II.5 Lattice Boltzmann methodology

The Boltzmann transport equation may be successfully solved using the Lattice Boltzmann method. Recent years have seen a significant increase in interest in this approach because of its many benefits for boundary resolution, effective management of the multi-scale coupling problem, and ease of programming. The single-mode LBM for phonon transportation is considered a solution of the BTE for estimating the distribution function of a representative phonon mode. Since only one representative mode with mean phonon properties is taken into account under the single mode approximation, all phonons are assumed to have the same relaxation time and velocity [6]. Since the purpose of this work is to employ the LBM for nano-heat transfer to address the thermal behavior of nano-scale transistors, the single-mode LBM was selected for the purposes of simplicity and clarity. The LBM discretizes the space domain by defining the lattice locations. The distribution functions in the LBM simulation move in the direction of the discrete velocity set assigned to the next lattice site at each time step. New distributions are then produced for each lattice site based on a set of collision principles[38, 44]. Eq. (II.5)'s derivative terms can be discretized in the manner shown below:

$$\frac{\partial e}{\partial t} = \frac{e(\mathrm{x}, t+\Delta t) - e(\mathrm{x}, \mathrm{t})}{\Delta t} \tag{II.7}$$

$$\frac{\partial e}{\partial \mathrm{x}} = \frac{e(\mathrm{x}+\Delta \mathrm{x}, t+\Delta t) - e(\mathrm{x}, \mathrm{t}+\Delta t)}{\Delta \mathrm{x}} \tag{II.8}$$

Equations (II.7) through (II.8) relate to the discrete energy distribution functions of phonons. Next, Eq. (II.5)'s discretization is provided by [34, 45] :

$$\frac{e_i(\mathrm{x}, t+\Delta t) - e_i(\mathrm{x}, \mathrm{t})}{\Delta t} + c_i \frac{e_i(\mathrm{x}+\Delta \mathrm{x}, t+\Delta t) - e_i(\mathrm{x}, \mathrm{t}+\Delta t)}{\Delta \mathrm{x}} = -\frac{e_i(\mathrm{x}, t) - e_i^{eq}(\mathrm{x}, \mathrm{t})}{\tau} + w_i q_v \tag{II.9}$$

Where $w_i$ stands for the weighting factor in each direction, x is the position vector, t is the time, ci is the discrete velocity, Δt is the time step, and Δx is the space step.

One can create the lattice space step and the time step by. This results in an LBM that generates heat internally; so, Eq. (II.9) may be recast as:

$$e_i(\mathrm{x}+\Delta \mathrm{x}, t+\Delta t) - e_i(\mathrm{x}, \mathrm{t}) = -\frac{\Delta t}{\tau}\left[e_i(\mathrm{x}, t) - e_i^{eq}(\mathrm{x}, \mathrm{t})\right] + \Delta t w_i q_v \tag{II.10}$$

The term $e_i\left(x, t\right)$ refers to the phonon's independent energy density, which is proportional to the phonon population associated with a specific lattice point. The discrete energy densities of the phonons in each direction of the lattice may be added together to determine the total energy density of the phonons[45].

$$e(\mathrm{x}, t) = \sum_{i=1}^{d} e_i(\mathrm{x}, t) = \sum_{i=1}^{d} e^{eq}(\mathrm{x}, t) \tag{II.11}$$

Assuming that the equilibrium phonon energy density is constant throughout all lattice directions, it may be computed using Eq. (II.11):

$$e_i^{eq}(\mathrm{x},t)=\frac{e(\mathrm{x},t)}{d} \tag{II.12}$$

## II.6 Lattice arrangements

In LBM, the terms "dimension" and "number of speed" are commonly expressed as $D_nQ_m$, where n stands for the problem's dimension (1 for 1-D, 2 for 2-D, and 3 for 3-D), and m for the speed model, or number of connections[44]:

### II.6.1 One-Dimensional:

The lattice utilized to describe the models $D_1Q_3$ and $D_1Q_2$ is shown in Fig. II.1:

**Fig II .3 :** Lattice arrangements for 1-D problems[44]

The discrete velocity set for $D_1Q_3$ is provided by:

$$\{c_0=(0,0)c, c_1=(1,0)c, c_2=(0,-1)c\} \tag{II.13}$$

When we do not take into account the particle (0) at rest, we refer to the model $D_1Q_2$. Discrete velocity is shown as follows:

$$\{c_1=(1,0)c, c_2=(0,-1)c\} \tag{II.14}$$

### II.6.2 Two-Dimensional:

The $D_2Q_9$ model is displayed in Fig. II.2, and the discrete velocity set is:

$$\begin{Bmatrix} c_0=(0,0)c, c_1=(1,0)c, c_2=(0,1)c, c_3=(-1,0)c, c_4=(0,-1)c, \\ c_5=(1,1)c, c_6=(-1,1)c, c_7=(-1,-1)c, c_8=(1,-1)c \end{Bmatrix} \tag{II.15}$$

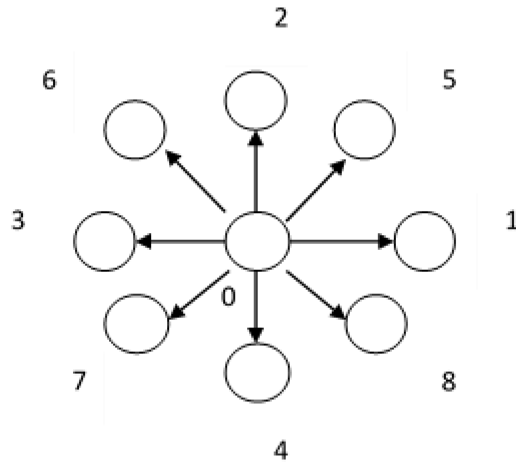



**Fig II.4:** Lattice model $D_2Q_9$ [48]

The $D_2Q_5$ model is displayed in Fig. II.3, and the discrete velocity set is:

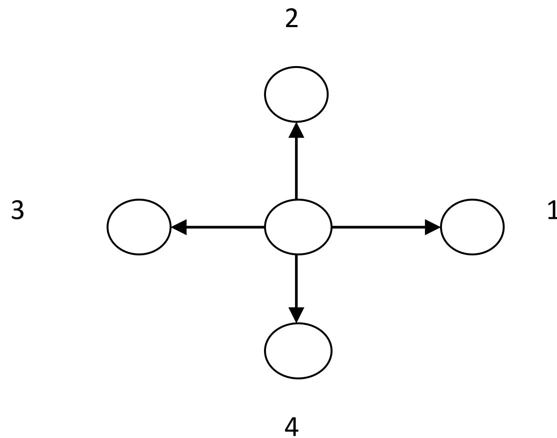



**Fig II.5:** Lattice model $D_2Q_5$[40]

$$\{c_0 = (0,0)c, c_1 = (1,0)c, c_2 = (0,1)c, c_3 = (-1,0)c, c_4 = (0,-1)c,\} \tag{II.16}$$

### II.6.3. Three-Dimensional:

Generally, $D_3Q_{15}$ and $D_3Q$= are the two models used to simulate three-dimensional issues.

$$c_i \begin{cases} (0,0,0)\,\mathrm{c} & \mathrm{i}=0 \\ (\pm1,0,0)\,\mathrm{c},(0,\pm1,0)\,\mathrm{c},(0,0,\pm1)\,\mathrm{c} & \mathrm{i}=1..6 \\ (\pm1,\pm1,0)\,\mathrm{c},(\pm1,0,\pm1)\,\mathrm{c},(0,\pm1,\pm1)\,\mathrm{c} & \mathrm{i}=7..18 \end{cases} \tag{II.17}$$

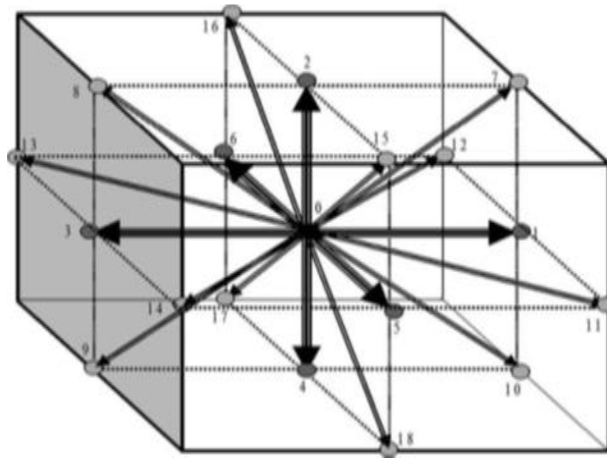



**Fig II.6:** Lattice arrangements for 3D problems, $D_3Q_{19}$[49]

$$c_i \begin{cases} (0,0,0)\,\mathrm{c} & \mathrm{i}=0 \\ (\pm1,0,0)\,\mathrm{c},(0,\pm1,0)\,\mathrm{c},(0,0,\pm1)\,\mathrm{c} & \mathrm{i}=1..6 \\ (\pm1,\pm1,\pm1) & \mathrm{i}=7..14 \end{cases} \tag{II.18}$$

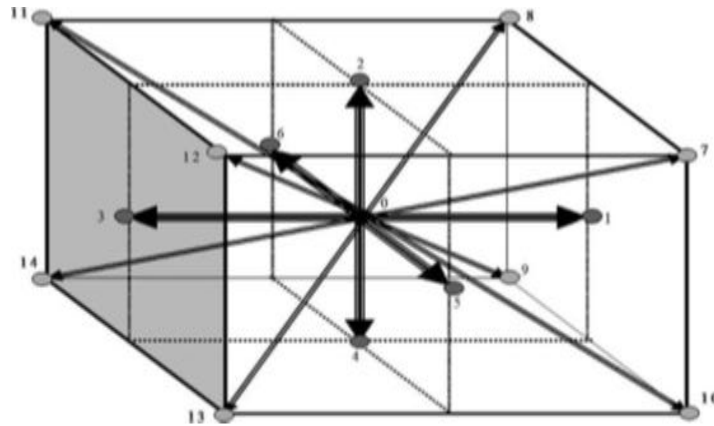


**Fig II.7:** Lattice arrangements for 3-D problems, $D_3Q_{15}$[5]

## II.7 LB M applications

Heat transfer, multiphase, hydrodynamic, and multi-component flows in porous media have all been expertly simulated by the LB technique [50 ،48]. A few domains where the LB approach is applied are depicted in Fig. II.8.

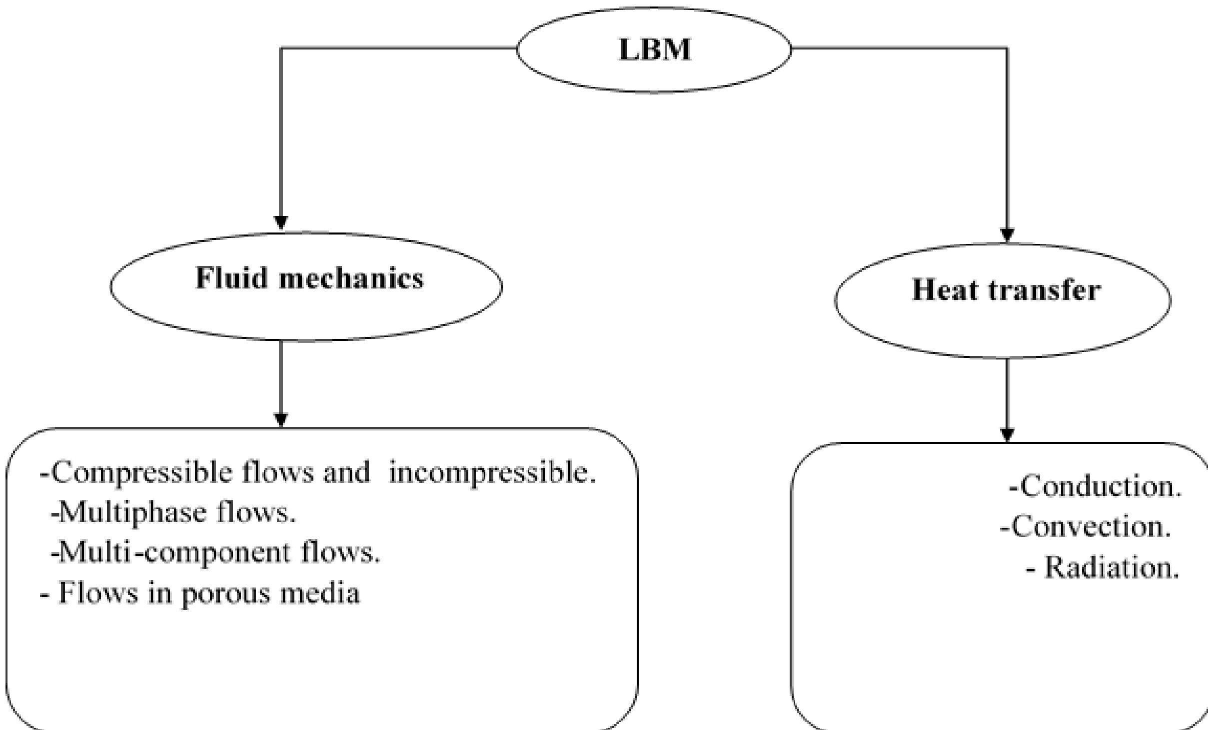



**Fig II.8 :** Different LBM application[44]

## II.8 Conclusion :

Numerical simulation utilizing various approaches is the topic of numerous research projects conducted globally. Instead of a mesh reflecting the structural domains and heat transfer, these techniques yield a set of control points that represent elementary volumes of matter that are tracked in their movement. For a very long time, the lattice Boltzmann method (LBM) has been used successfully to simulate fluid flows and transport phenomena. As opposed to traditional techniques like CFD.

# Chapter III: Investigation of heat conduction in MESFET nanodevice

## III.1. Introduction

The reduction in structural dimension to the mean free path of material with phonon scattering at the border influences the heat conduction process, and particle vibration (phonon) frequently limits thermal transfer inside a nanoscale domain [51]. The bulk is modeled using thermal conductivity in the phonon Boltzmann transport process model, where the ETC is correlated with the Knudsen number [52]. Thus, we can express the length-dependent ETC over the channel device system as follows [53-55]:

$$k_e(Kn) = k\left[1 - \frac{2\times Kn\times \tanh(1/(2\times Kn))}{1 + c_p\times \tanh(1/(2\times Kn))}\right] \qquad \text{(III.1)}$$

In this case, cp = 2(1+p)/(1-p), where p is the specularity parameter, which is defined as the probability of the phonon scattering process at the border. The constants Kn and cp are related to the Knudsen number and the characteristic of the material, respectively [18, 56]. Furthermore, the relaxation time related to the border phonon scattering is defined as[40, 55]

$$\tau_b = \frac{3\times k_e}{C\times v^2} \qquad \text{(III.2)}$$

Eq. (II.5) in this instance expressed as fellow:

$$\frac{\partial u}{\partial t} + v.\nabla u = -\frac{u - u^{eq}}{\tau_b} + q_v \qquad \text{(III.3)}$$

Thus, the non-dimensional version of Eq. is as follows:

$$u_i^*(x^* + \Delta r^*, t^* + \Delta t^*) - u_i^*(x^*, t^*) = -\frac{\Delta t^*}{\tau_b^*}\left[u_i^*(x^*, t^*) - u_i^{eq*}(x^*, t^*)\right] + w_i q_v^* \qquad \text{(III.4)}$$

## III.2. Description of structure:

The source and drain electrodes of a MES transistor are electrically coupled to a gate and a layer channel[57, 58].The simulation designs for the study recommended by the mesoscopic approach are shown in Fig. III.1 The structure of a MES transistor device is seen in Fig. III.1. This work considers the device sizes: L = 100 nm and l =50 nm with a heat generating area of 10 nm×10 nm. It is assumed that the active channel of nanotransistors generates heat continuously ($qv=10^{19}$ $W/m^3$). Table III.1 lists the materials' used thermal properties for the numerical simulation . The heat transfer simulation described in this work was performed using the adopted lattice Boltzmann method implemented in the Fortran programming. Common features of LBM, collision and dispersion, different boundary conditions, and computation of value variables are applied .

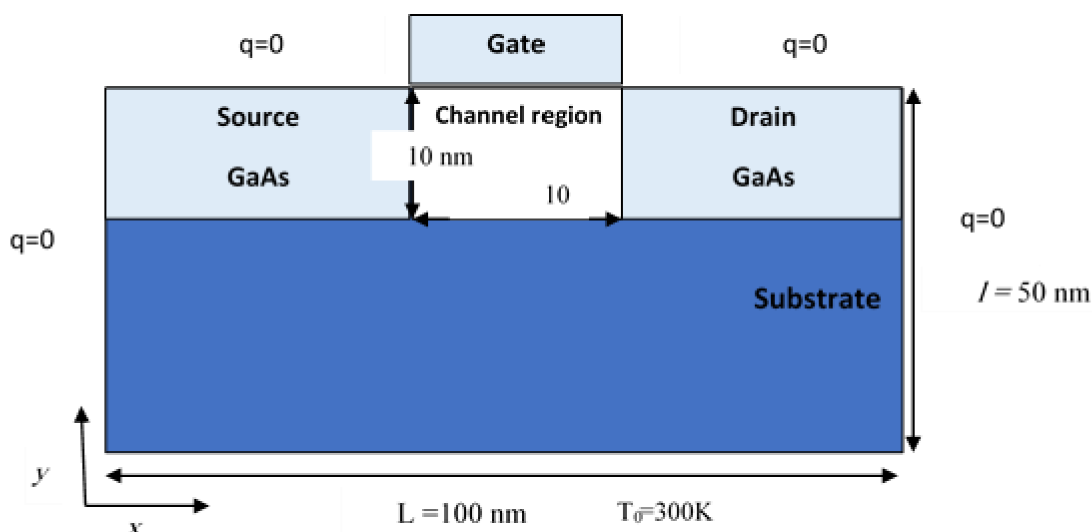



**Fig III.1:** A GaAs – MESFET nanodevice.

**Table III.1:** Heat features of Silicon dioxide ($SiO_2$), GaAs , and Silicon (Si)

| Substrate | k ($W. m^{-1}K^{-1}$) | Λ (nm) | C ($J. m^{-3} K^{-1}$) |
|---|---|---|---|
| Si | 150 | 100 | $1.55\times10^6$ |
| GaAs | 50 | 5.8 | $1.86\times10^6$ |
| $SiO_2$ | 1.4 | 0.4 | $1.75\times10^6$ |

## III.3. Simulation results and discussion:

In the present work, a study on the sub-continuum 2D heat transfer within nanoscale MESFET for different substates is reported employing the LBM $D_2Q_8$ model.

Fig III. 2 presents the curves of evolution a comparison of temperature with time for different substrate materials Si ,GaAs ,$SiO_2$ at the time scale t=30 ps. It noticed that the nano-MES transistor,

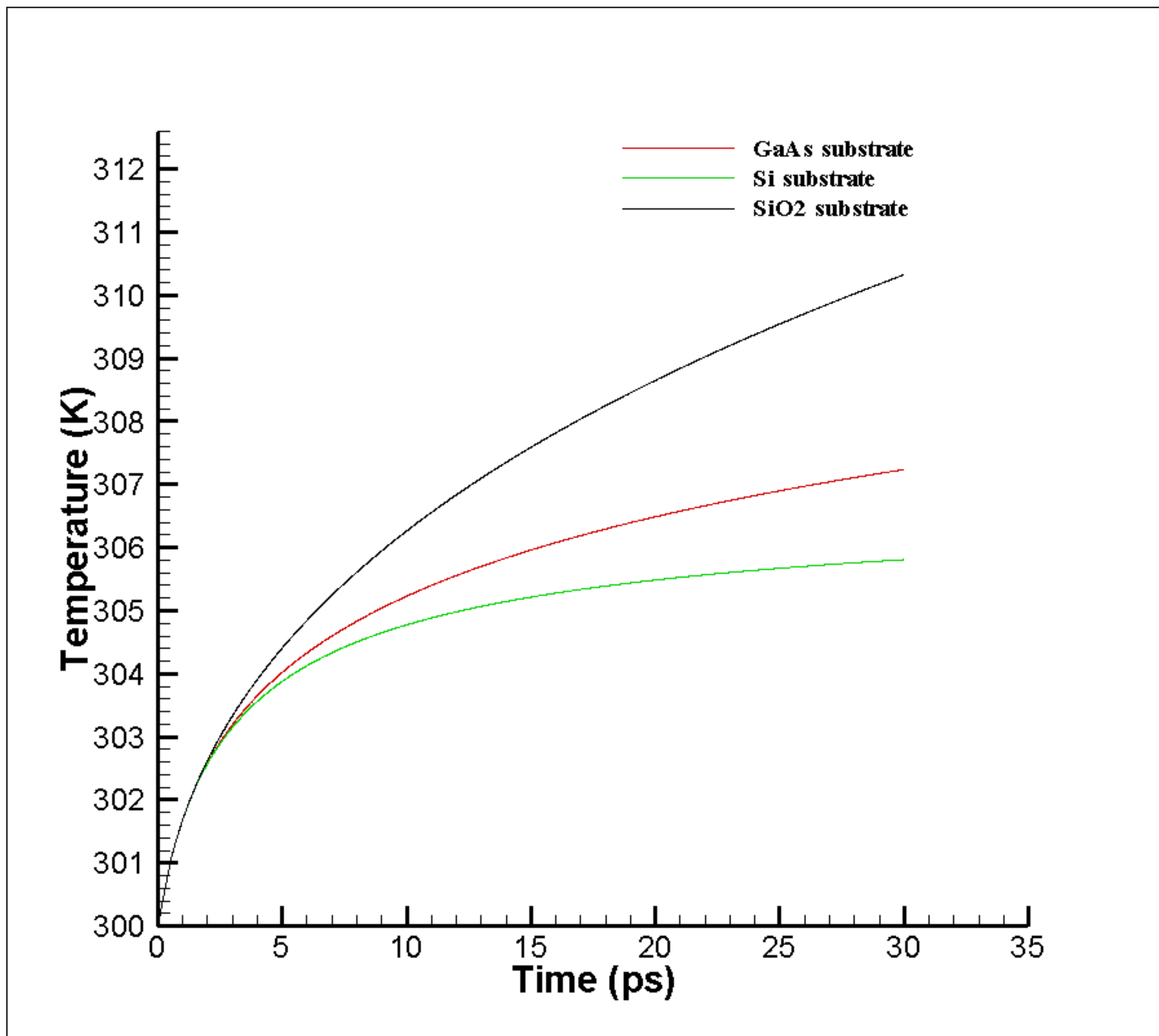



Fig III.2: Evolution temporal temperature of MESFET for different substrate at p =0.3.

which is manufactured on silicon, is more stable (low temperature) than the rest of the materials as the temperature is estimated. 305 K, followed by GaAS at 307.4 K, and $SiO_2$ transistor at 310.6 K due to silicone's high thermal conductivity compared to other materials.

The following graphic curves represent temperatures change with time and different substrate materials Si ,GaAs at p = 0.3 and p = 0.6 as shown in Fig III.3 . It located that the temperatures are increased with time for both substrate materials, but we notice that the temperatures for the specularity coefficient p = 0.6 is lower than p=0.3 over time. Comparison between these two substrates models show the temperature rises when the reflectivity parameter decreases because of effect of specularity parameter on thermal coductavity value for various materials.

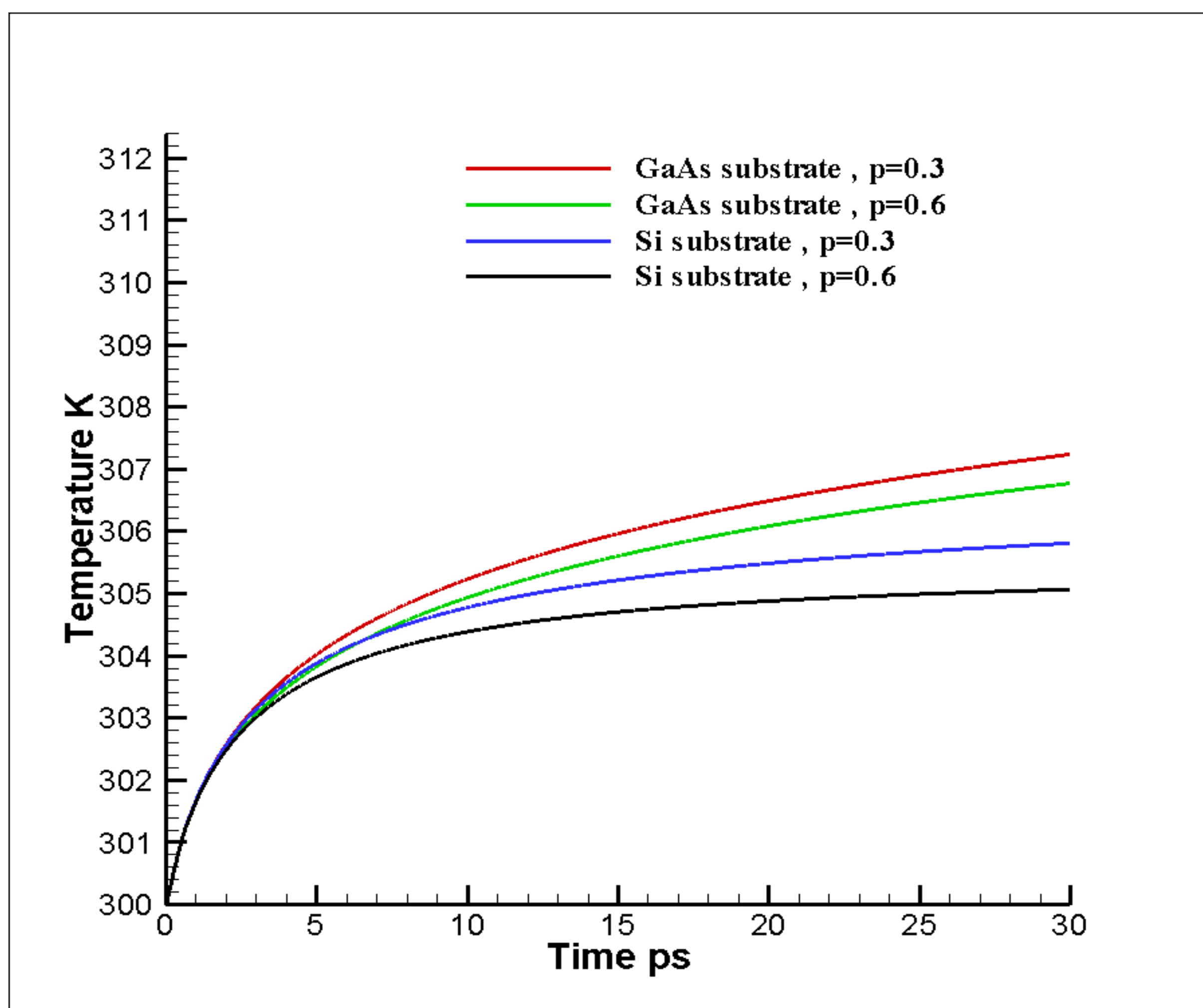



Fig III.3: Evolution temporal temperature of MESFET for different substrate and specularity factor.

Fig III. 4 shows graph of change in temperatures on function of the y-direction at the center line of a nanodevices in terms of different materials (Si ,GaAs and $SiO_2$) at p = 0.3 and p = 0.6 and the current model (y < 5 0nm). We note that the $SiO_2$ material is more hotspots. The temperature in both reflectivities, p = 0.3 and p = 0.6, exceeds 310 K at y = 38 n m, followed by GaAs, which exceeds 305 K at y = 40 n m. The Si material comes in good, as it exceeds 305 K at y = 40 n m, which is the least heat absorption, y = 40 n m, and also the lower the reflectivity coefficient, the less heat transfer.

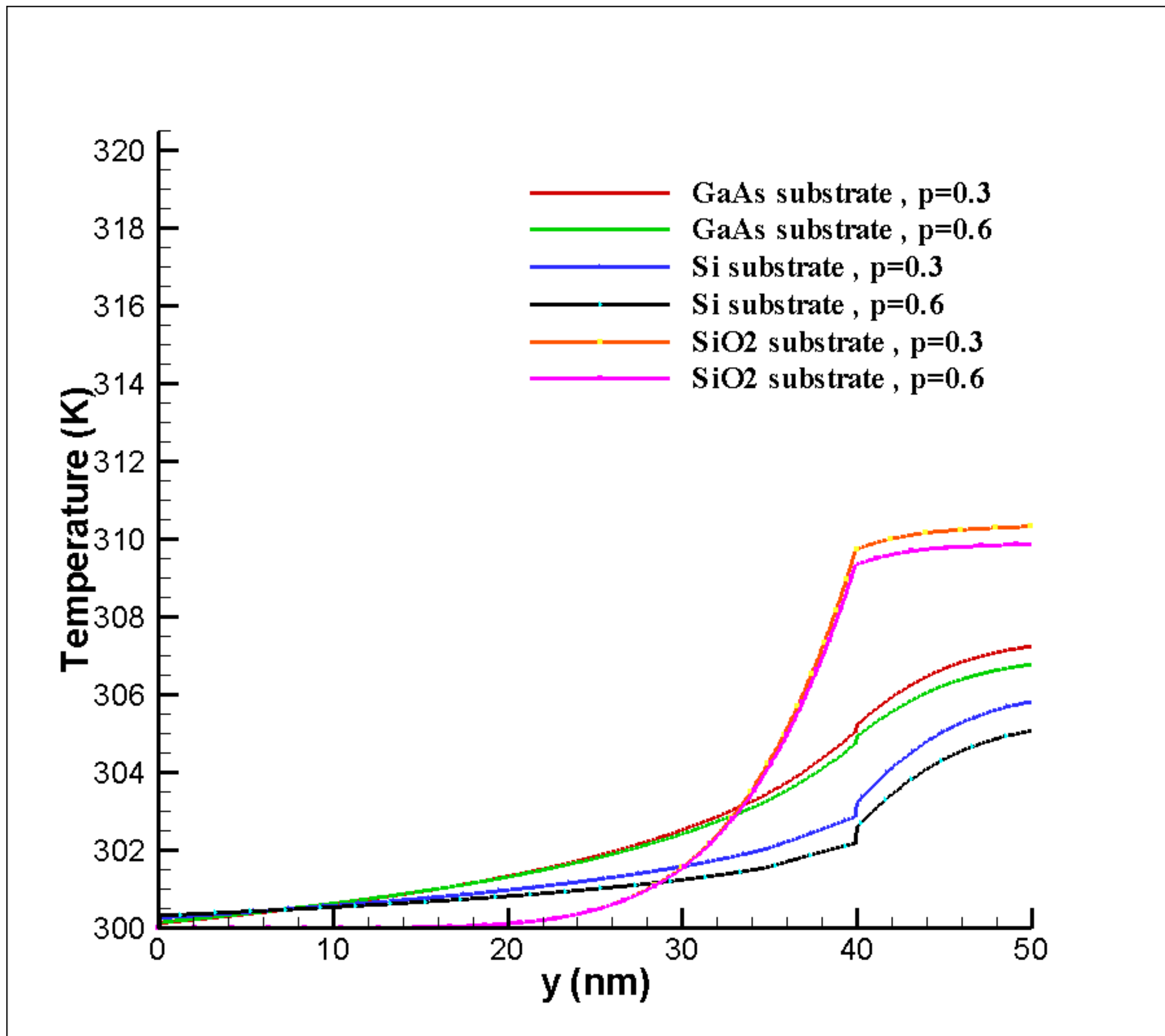



Fig III.4: Temperature profiles along y-direction in the centerline of MESFET with Si,$SiO_2$, GaAS at p=0.3and p=0.6 .

Fig III .5 shows the temperature relation for nanoscale transistors at y = 0 for various periods plotted against the x direction. With regard to the centerline axis, the curves' shapes are symmetrical. The results show that there are detectable hot spots in the active zone because of the heat produced by Joule (electron particle) impact and that the greatest hot spot is situated near the center line and expands with time. Within a silicon transistor, the highest temperatures for SIO2 are 306.4 K and 310 K at 10 ps and 30 ps, respectively. The highest temperatures are

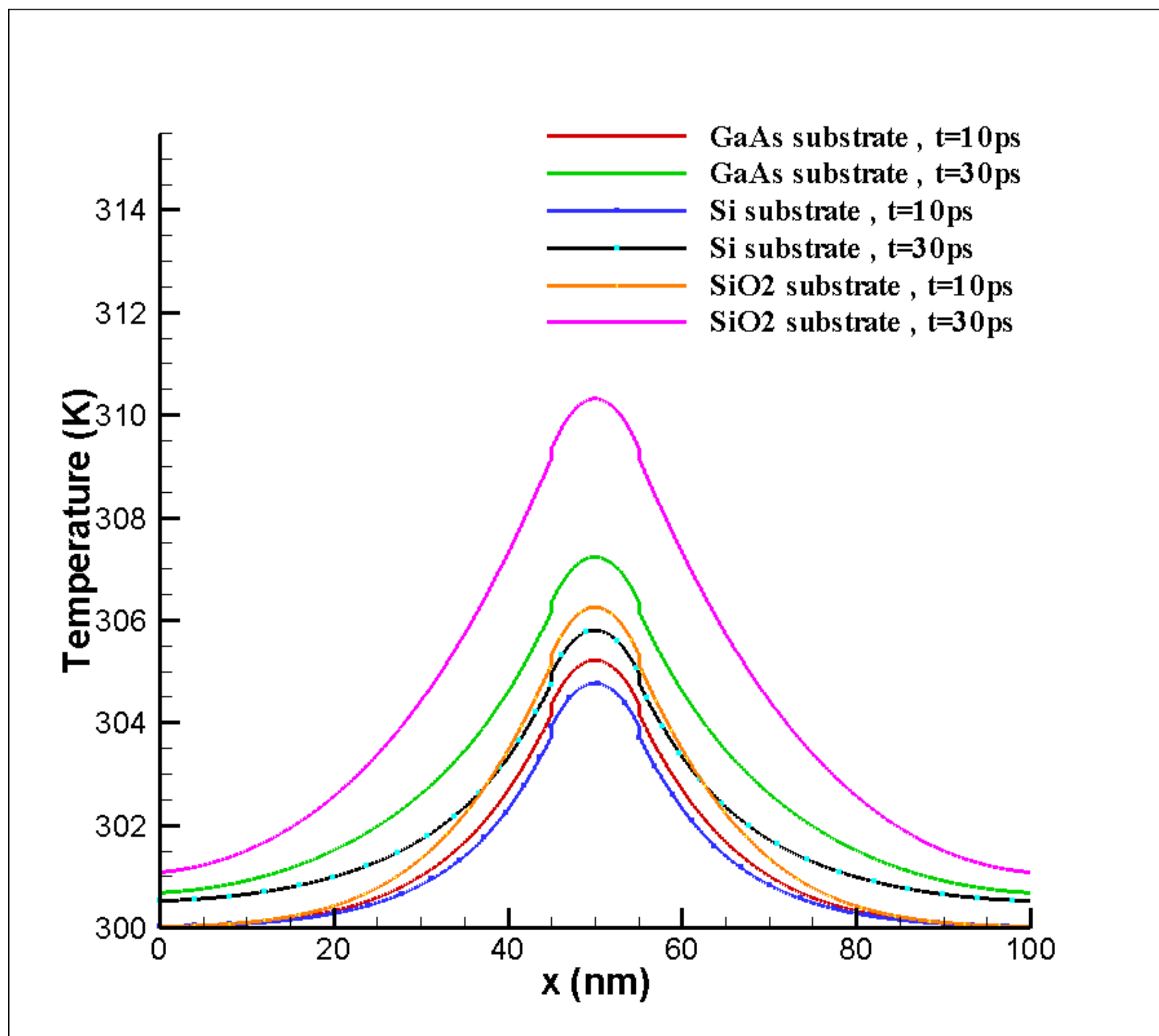



Fig III .5: Evolution temperature versus x-axis of the MESFET for different substrate Si, GaAs and $SiO_2$ and time at y = 50 nm.

304.4 K and 304.9 K for Si at 10 ps and 30 ps, respectively. The highest temperatures for GaAs are 304.6 K and 307 K at 10 ps and 30 ps, respectively. Because graphene has a higher thermal conductivity than silicon, which has a lower one, there is a difference in the maximum hot spots.

The following graph represents the temperature changes in Kelvin as a function of the y-axis on the center line of the transistor in terms of different substrate materials as presented in Fig III.6.At t=10ps t=30ps and the current model (y < 50 nm),we notice that there is a significant increase in temperature starting from y = 30 nm for all materials, and the higher the value of time , the higher the temperature, meaning that there is a direct related between time and temperature.

at

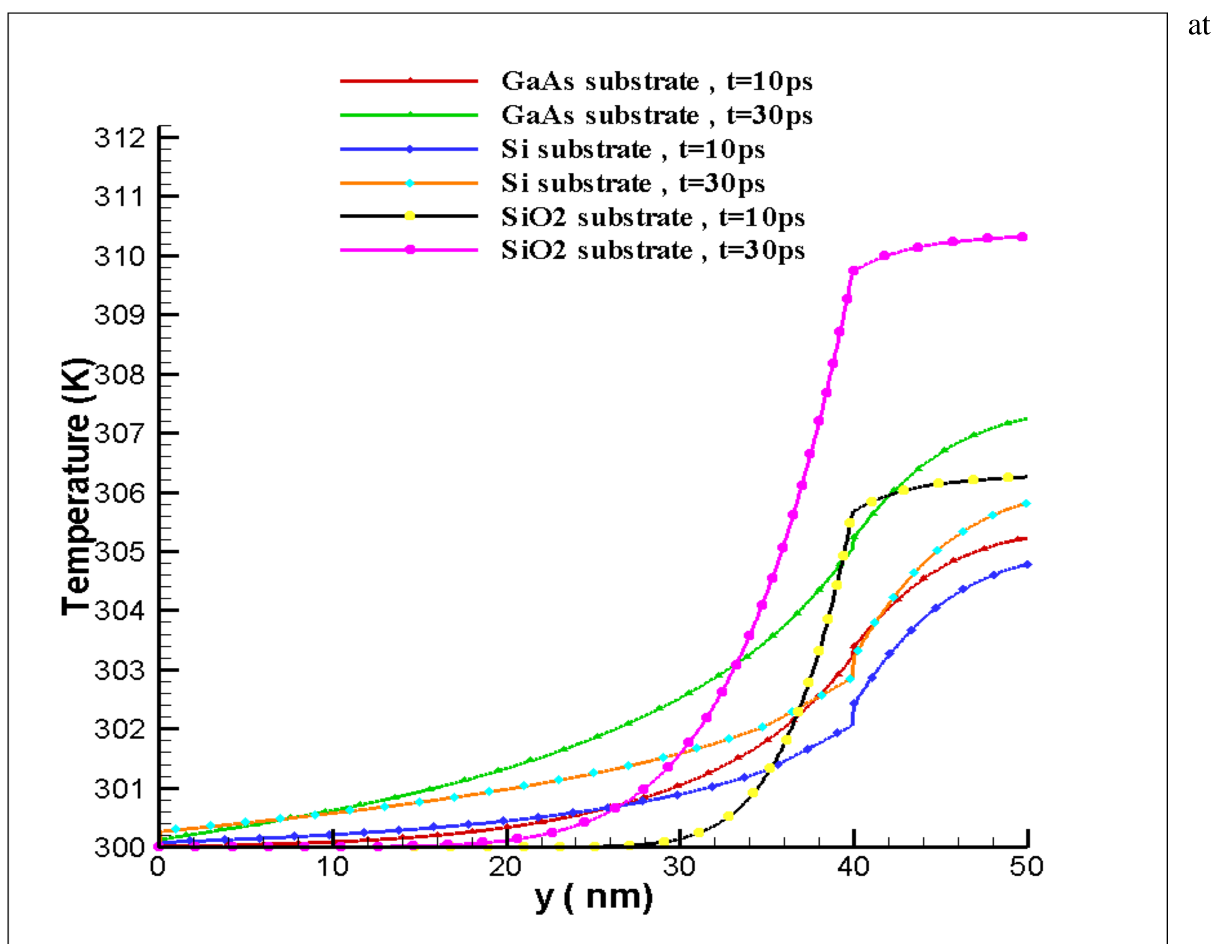
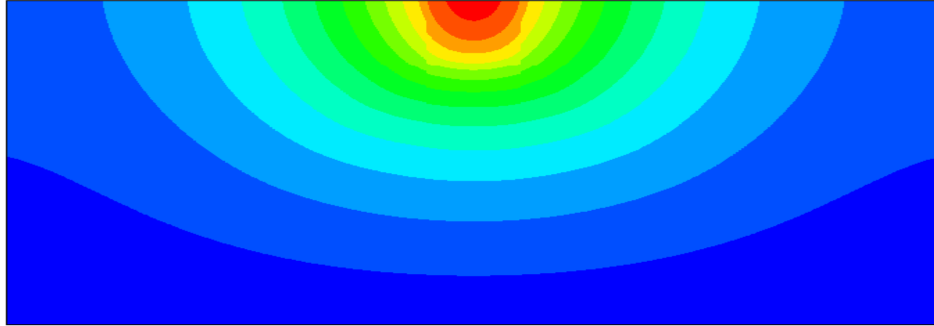
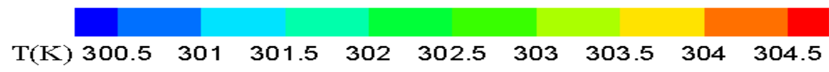
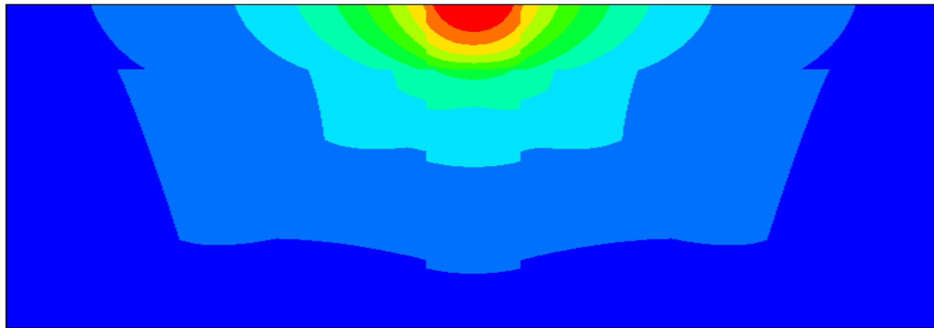



Fig III.6 Evolution temporal temperature difference of nanotransistor for different substate at *x*=*L*/2 , (*p*=0.3)

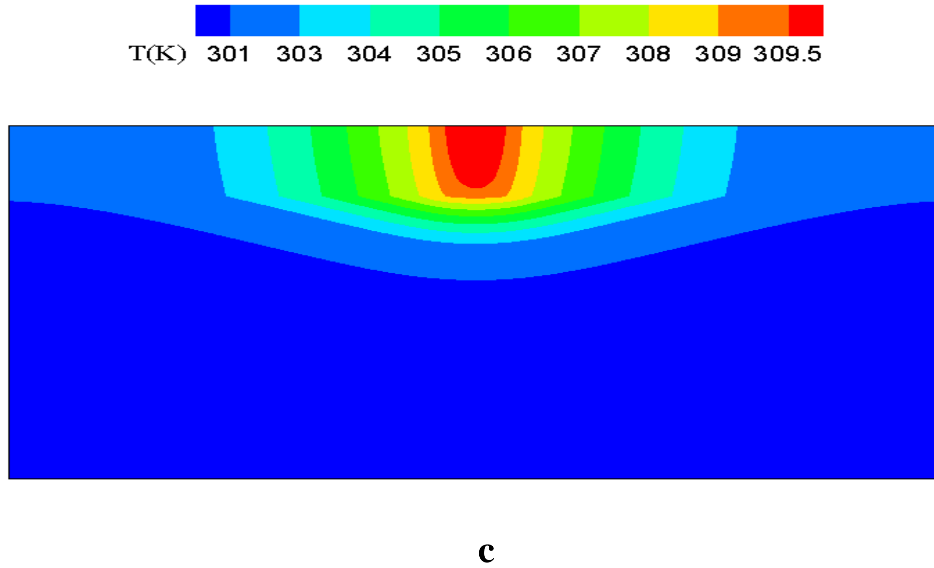


**a**



**b**




**c**

Fig III. 7 :2D temperature distribution in MESFET for different substrates at p=0.6 and t=30ps

a) GaAs, b) Si , c)$SiO_2$

Fig. III. 7 shows the 2D impacts of the substrate materials on the temperature distribution at p = 0.6 and t = 30 ps. It is clear that for each of the three substrates, the temperature maintains symmetry with respect to the MES transistor's centerline (x=L/2). The left and right of the active zone exhibit an increase in heat dispersion, as depicted in these pictures. The buried oxide layer functions as a heat cage, preventing heat from entering the substrate and leading to a notable temperature increase inside the transistor. This makes it clear in Fig. III. 7(c) that the temperatures are confined in the source-drain. While Figs. III. 7(a) and (b) demonstrate that the majority of heat exits the transistor to the bottom, this phenomena has an impact on the electrical transport in the nano-device.

## III.4 Conclusion

The primary goal of this work is to calculate the heat transfer in a 2D sub-length 100 nm MES transistor with a distinct substrate while taking into account the integrated LBM $D_2Q_8$ model with specularity factor in the thermal area in the presence of a permanent heat source. Three substrates that matched the real conditions were used to evaluate the results. Compared to other modeling approaches, the model suggested in this paper has the benefit of accounting for phonon transport with the collisional phonon in sub-continuum modes. It is believed that these simulation results would aid other researchers in comprehending the mechanism by providing insights into the heat behavior inside nanotransistors when substrates with the specularity factor are present.

## Conclusion general

This work's main goal is to investigate how temperature behavior affects nanoelectronic devices. Several simulation experiments with the lattice Boltzmann method under parameter influence have been carried out to comprehend this transport phenomenon. The following can be used to finish the study's organization: The first chapter provides an overview of transistor electronic device technology, including topics such as the device's multiple forms, operation, developmental stages, size, and several prior research projects. The Lattice Boltzmann approach was selected in Chapter two for a number of reasons, including its great computing efficiency, ease of programming, parallelization, and unambiguous mathematical and physical modeling. This technique is capable of integer. Boundary conditions can be implemented in this geometry and integer structure can be achieved using this method. The simulated results using the LBM model that was used in Chapter Three are shown.

The simulation results showed the devices with different substrate, where it was observed that the temperature increases with time in a direct relationship. On the other hand, we note that there is a positive effect in increasing the reflectivity coefficient in reducing the temperature for devices studied. On the other hand, we note that There is thermal diffusivity on the right side and the left side of the conveying channel, and there is also diffusivity at the bottom of the conveying channel .The temperature in both reflectivities, $p = 0.3$ and $p = 0.6$, exceeds 310 K at $y = 38$ nm, followed by GaAs, which exceeds 305 K at $y = 40$ nm. The Si material comes in good, as it exceeds 305 K at $y = 40$ nm, which is the least heat absorption, $y = 40$ nm, and also the lower the reflectivity coefficient, the less heat transfer.

The obtained results suggest that the reflectivity coefficient (p) has a significant effect in both lowering the electronic device's maximum temperature and phonon heat transmission. Future nanoelectronic systems could benefit greatly from the particular features of silicon materials and the device preference of silicon substrate. Due to the material's special qualities and the benefits of silicon transistor devices, silicon is a viable option for upcoming nanoscale device systems.

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