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Thesis

Defect effect on the electric characteristics of Schottky contacts

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﴿ رَبَّنَا لاَ تُؤَاخِذْنَا إِن نَّسِينَا أَوْ أَخْطَأْنَا رَبَّنَا وَلاَ تَحْمِلْ عَلَيْنَا إِصْرًا كَمَا حَمَلْتَهُ عَلَى الَّذِينَ مِن قَبْلِنَا رَبَّنَا وَلاَ تُحَمِّلْنَا مَا لاَ طَاقَةَ لَنَا بِهِ وَاعْفُ عَنَّا وَاغْفِرْ لَنَا وَارْحَمْنَا أَنتَ مَوْلاَنَا فَانصُرْنَا عَلَى الْقَوْمِ الْكَافِرِينَ﴾ **سورة البقرة : الآية286 .**

" صدق الله العظيم"

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First of all, I thank Almighty God -ALLAH- for giving me courage and patience during all these years of study.

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We would like to sincerely thank all those who have helped us to elaborate and carry out this dissertation, as well as to all those who have helped us directly or indirectly to accomplish this work.

Finally, I especially thank my parents for their unconditional support throughout these long years of study.

DEDICATION

In the name of God, the Merciful Praise be to Allah Almighty

We dedicate this humble work as respect, appreciation and thanks:

To our dear fathers, mothers and brothers who helped us from near and far.

To everyone who contributed to the development of this humble work and all these are dear to us.

Abstract

الملخص

Abstract

This thesis investigates the impact of defects on the electrical characteristics of Schottky contacts. It begins with an overview of semiconductor physics and the formation of metal–semiconductor junctions. Various methods are analyzed to extract key diode parameters such as the Schottky barrier height and ideality factor. Simulations using Atlas-Silvaco are conducted to model the influence of defects and temperature on diode behavior. The results show that defects lead to notable deviations from ideal characteristics, including increased ideality factor and barrier inhomogeneity. A comparative study of MS and MIS structures highlights the critical role of interface quality. This work contributes to a better understanding of defect-related effects and supports the design of more efficient Schottky-based devices for modern electronic systems.

Keywords: Semiconductor, the barrier height, Schottky.

الملخص

تبحث هذه المذكرة في تأثير العيوب على الخصائص الكهربائية لوصلات شوتكي. تبدأ بعرض لمبادئ فيزياء أشباه الموصلات وتكوين وصلة معدن-شبه موصل. تم تحليل عدة طرق لاستخلاص المعلمات الأساسية للديود مثل ارتفاع حاجز شوتكي وعامل المثالية. تم إجراء محاكاة باستخدام برنامج **Atlas-Silvaco** لنمذجة تأثير العيوب ودرجة الحرارة على سلوك الديود. أظهرت النتائج أن العيوب تؤدي إلى انحرافات ملحوظة عن السلوك المثالي، مثل زيادة عامل المثالية وعدم تجانس الحاجز. كما أظهرت الدراسة المقارنة بين هياكل **MS** و**MIS** الدور الحاسم لجودة الواجهة. تسهم هذه الدراسة في فهم أفضل لتأثيرات العيوب وتدعم تصميم أجهزة شوتكي أكثر كفاءة للتطبيقات الإلكترونية الحديثة.

الكلمات المفتاحية: أشباه الموصلات، ارتفاع الحاجز، شوتكي.

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General Introduction

General Introduction

The continuous evolution of modern electronic devices has intensified the need for high-performance, energy-efficient, and miniaturized components. Among the key elements in micro- and nanoelectronics are Schottky contacts, which form the interface between a metal and a semiconductor. Due to their fast switching behavior, low forward voltage drop, and high-frequency response, Schottky diodes have found widespread applications in power rectification, RF circuits, and photovoltaic systems. However, the electrical characteristics of these contacts are highly sensitive to structural and interfacial imperfections—particularly to the presence of defects. These defects, whether originating from impurities, dislocations, interface states, or inhomogeneities in the barrier, can significantly alter the transport mechanisms, barrier height, ideality factor, and leakage current, leading to deviations from ideal behavior.

This thesis aims to investigate the influence of defects on the electrical performance of Schottky contacts, with a specific focus on the variation of extracted parameters and simulation results under different conditions. To lay the groundwork, Chapter I presents the fundamental properties of semiconductors and the physical principles governing Schottky barrier diodes. It discusses the ideal and non-ideal behaviors and the factors that affect carrier transport across the metal–semiconductor interface. Chapter II reviews the main experimental and theoretical techniques used to extract key diode parameters, such as the barrier height, ideality factor, and series resistance. These techniques are essential for diagnosing the impact of defects and understanding their electrical signatures. Finally, Chapter III provides detailed simulation results using advanced tools to model the diode behavior in the presence of defects, allowing for a comparative analysis between ideal and defect-influenced structures.

Finally, we conclude our work with a general conclusion and perspectives.

Through this work, a deeper understanding of how material imperfections affect Schottky contact performance is developed, which is crucial for the design and optimization of reliable semiconductor devices in future electronic systems.

Chapter I

Basic properties of Semiconductor and Schottky barrier diode

I.1. Introduction

Because of their special electrical characteristics, semiconductors a crucial field of research in material science have revolutionized modern technology. By creating semiconductors with remarkable mechanical, chemical, and physical properties, material scientists have made important contributions.

The Schottky diode is a surface contact of a metal with a semiconductor, the first diodes were discovered by F. BRAUN in 1874 [1], although very old, but they remain the research study until today thanks to its many applications.

In fact, Schottky diodes have been widely used for a wide variety of applications such as solar cells, photo detectors, Schottky transistors, microwave mixers, Zener diode and various integrated circuits, the Schottky diode can also be used as a variable capacitor in parametric circuits for frequency multiplication [1-2]

I.2. The Concept of semiconductor

Depending on the external factors they are exposed to, such as temperature, pressure, radiation, magnetic or electric fields, semiconductors can act either as conductors or insulators [1].

Semiconductors are crystalline materials with average electrical conductivity, allowing them to function as both a conductor and an insulator. 14 semiconductor elements are listed in the periodic table, including silicon, germanium, selenium, cadmium, aluminium, gallium, boron, indium, and carbon.

According to the band theory, the highest energy band allowed (the valence band) is entirely occupied by electrons in semiconductors. However, the height of the forbidden band of a semiconductor is low (1eV), whereas it is remarkable for the true insulators, and is situated between this entire band and the first band upper vacuum in the energy diagram (conduction band) [2].

Most semiconductor materials are single crystals. Figure I.1 exhibits three cubiccrystal unit cells - simple cubic, body-centered cubic, and face-centered cubic.

The element semiconductors, silicon and germanium, have a diamond lattice structure as shown in Figure I.2. This configuration belongs to the cubic-crystal family and can be envisaged as two interpenetrating fcc sublattices with one sublattice staggered from the other by one quarter of the distance along a diagonal of the cube. All atoms are identical in a diamond lattice, and each atom in the diamond lattice is surrounded by four equidistant

nearest neighbors that lie at the corners of a tetrahedron. Most of the III-V semiconductors (e.g. GaAs) have a zincblende lattice (shown in Figure I.2b) that is identical to a diamond lattice except that one fcc sublattice has Column III atoms (Ga) and the other has Column V atoms (As).

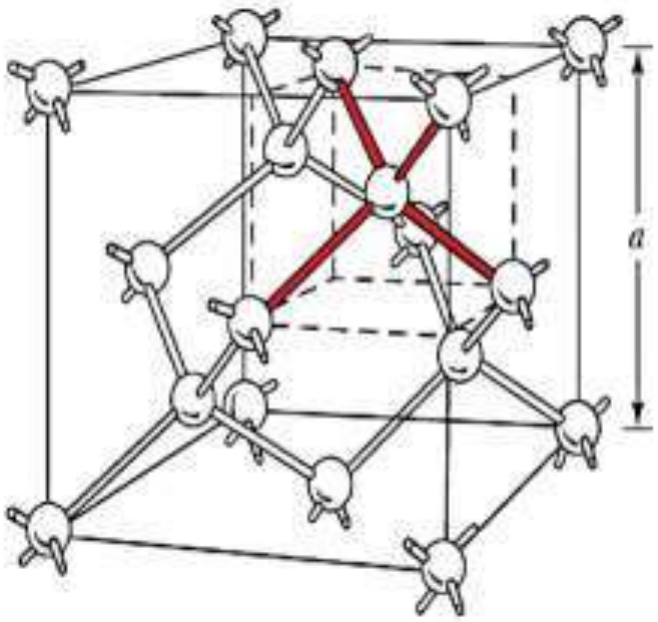


Figure I.1: Diamond lattice

I.3.Electrical conductivity in semiconductors

Figure (I.2) illustrates the electrical conductivity of several materials at room temperature. The conductivity of semiconductors is restricted at room temperature and falls between that of metals and insulators. At absolute zero, they behave as insulators. Their electrical characteristics can be altered by doping them with impurities or altering the temperature [3].

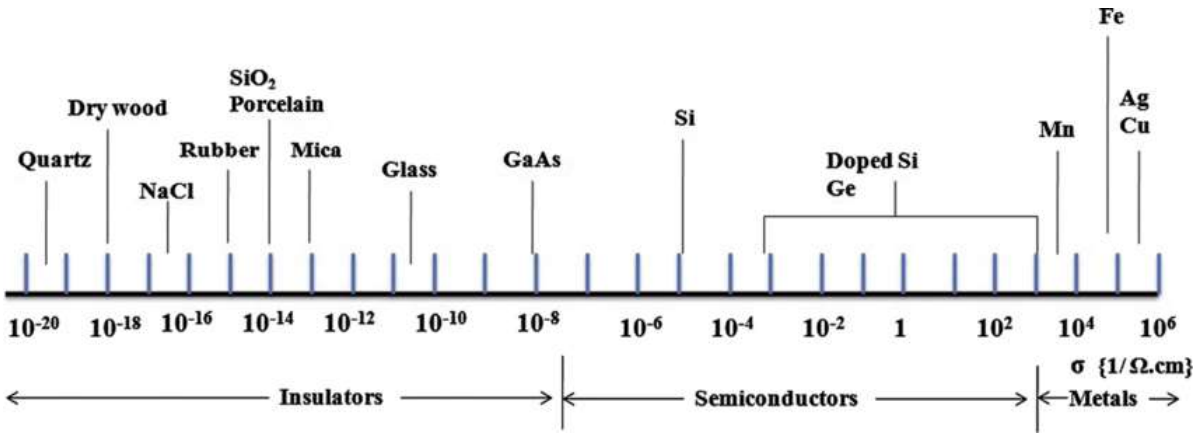


Figure I.2: Electrical conductivity at room temperature of some types of materials [2].

I.4. Energy Bands

The process of creating a diamond lattice crystal from separate silicon atoms is shown schematically in Figure I.3. As the two atoms get closer to the equilibrium interatomic distance, the energy band separates into the valence band and the conduction band. The region separating the conduction and valence bands is termed the forbidden gap or bandgap, E_g. The energy band diagrams of the three kinds of solids insulators, semiconductors, and conductors are shown in Figure I.4. Because of the comparatively high bandgap in insulators, the topmost electron in the valence band cannot be raised to the conduction band by thermal energy or an applied electric field. There is no bandgap and current flows easily in metals and conductors because the conduction band is either fully filled or overlaps the valence band [5].

In semiconductors, the bandgap is smaller than that of insulators, and thermal energy can excite electrons to the conduction band. The bandgap of a semiconductor decreases with higher temperature. For instance, for silicon, E_g is 1.12 eV at room temperature and 1.17 eV at zero Kelvin.

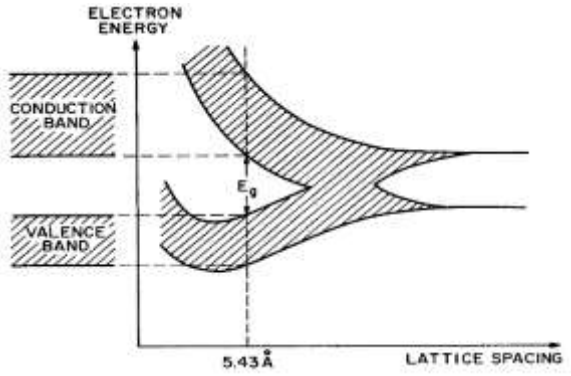


Figure I.3: Formation of energy bands as a diamond lattice crystal by bringing together isolated silicon atoms[5].

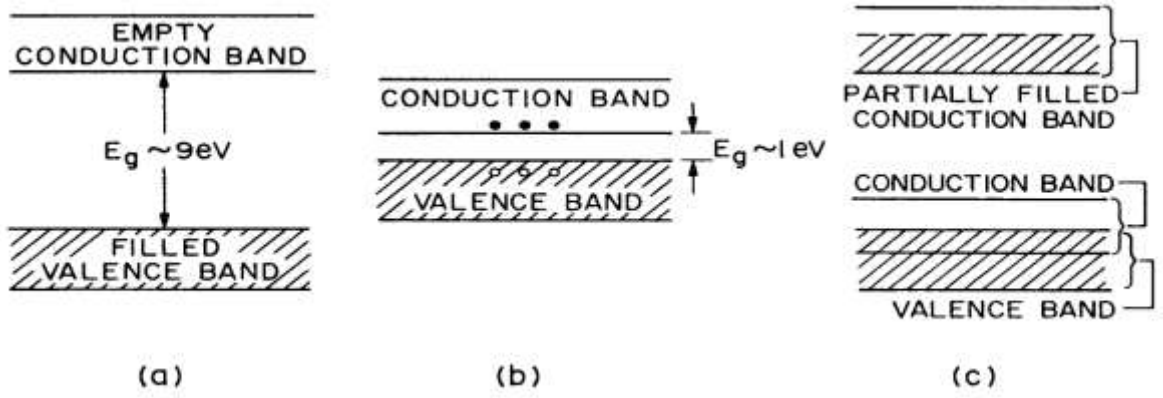


Figure I .4: Schematic energy band representations of (a) an insulator, (b) a semiconductor, and (c) conductors[5].

Figure I.5 shows a more detailed schematic of the energy band structures for silicon .

Silicon have an indirect bandgap semiconductor as a change in crystal momentum is required for an electron transition between the valence and conduction bands.

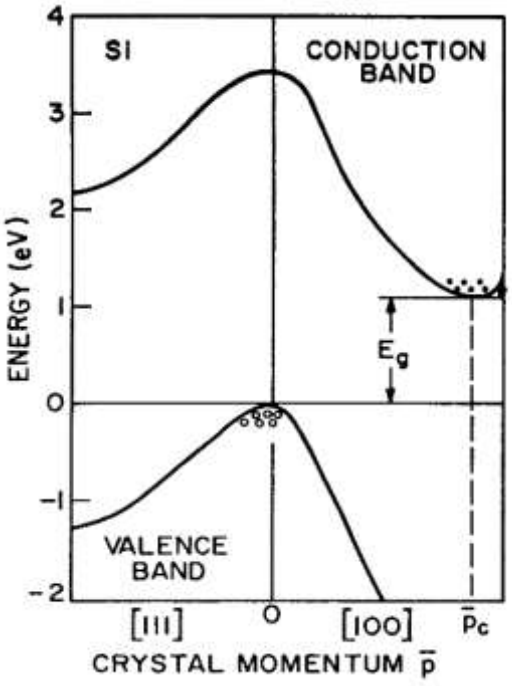


Figure I.5: Energy band structures of Si [5].

I.5. Types of semiconductors

We distinguish between two types of semiconductors: doped extrinsic and perfect intrinsic semiconductors.

I.5.1. Intrinsic semiconductors

They have a very low level of impurities and are extremely pure and wellcrystallized semiconductors with a fully periodic crystalline lattice (less than 1 impurity atom for 10^13 atoms of the semiconductor element). At very low temperatures, they act as insulators and their conductivity increases with the increase of temperature. We call a semiconductor intrinsic if the electrons number n in the conduction band is equal to holes' number p in valence band [7].

I.5.2. Extrinsic semiconductors

Doping an intrinsic semiconductor doped by specific impurities makes it extrinsic, while keeping the initial purity level well above the doping rate. Depending on the nature of the atoms introduced, the number of electrons becomes much greater than the number of

holes so the semiconductor is called type n, either the number of holes becomes much higher than that of electrons or the semiconductor is called type p.

I.5.2.1.N-type semiconductors

By introducing penta-valent atoms such as phosphorus P, arsenic As into a crystal, some bonds are blocked giving way to these extra atoms which have five valence electrons which fills the bonds by leaving a free electron in the crystal not closely linked to the nucleus (E 0.01eV), and passes easily into the conduction band. Penta-valent or donor atoms become positive ions after the excess electrons pass through the conduction band [4].

This greatly increases the conductivity of the doped material. Negative charges (electrons) are said to be the majority.

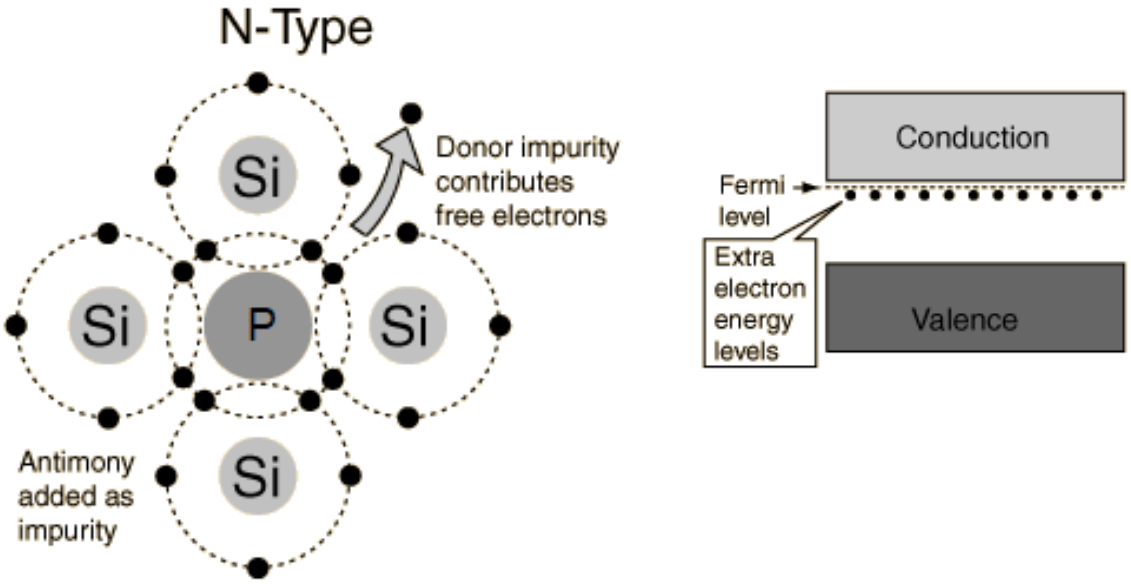


Figure I.6: N-type Semiconductor [4]

I.5.2.2. P-type semiconductors

In this case we introduce trivalent atoms such as Gallium Ga, Indium In, boron B, aluminium Al. The impurity is missing a valence electron to ensure the 4 bonds with the neighboring silicon atoms. A low energy input (0.05eV) is enough for an electron of nearby silicon to be captured by the impurity: there is formation of a hole that is loosely bound and therefore mobile. The trivalent atoms (acceptors) become negative ions by capturing an electron. Considering the doping rates. These holes are much more numerous than the intrinsic carriers of pure crystal. The extrinsic conduction type p (positive) increases and is ensured by holes, the holes become majority [4].

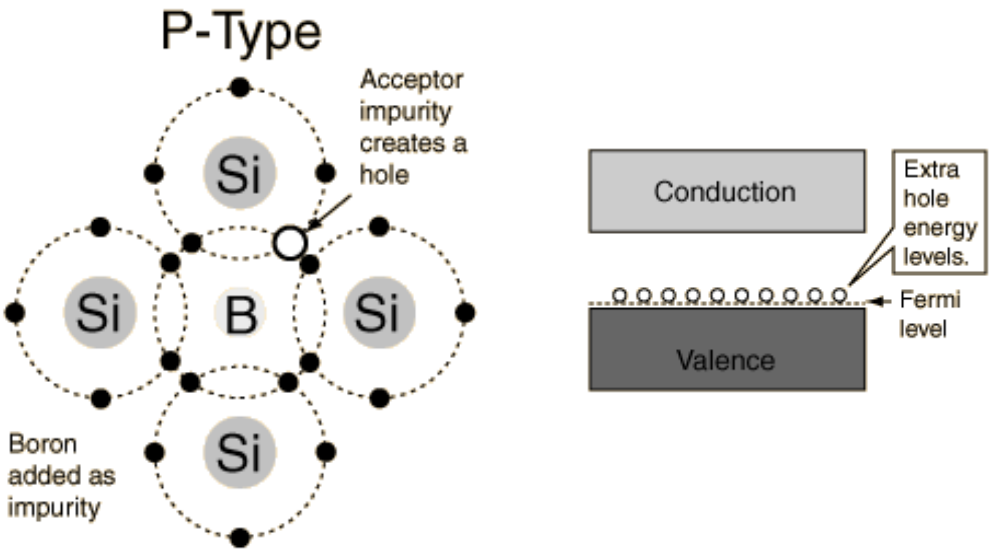


Figure I.7: P-type Semiconductor [4]

I.6. Classification of semiconductors

Semiconductors are classified according to their chemical composition and stoichiometry.

I.6.1. Elementary semiconductors

There are elementary semiconductors such as silicon (Si), the germanium (Ge) and grey tin (a - Sn), which belong to Group IV of the periodic table.

I.6.2. II -VI semiconductors

There are also II -VI semiconductors combining the elements II (Be, Mg, Ca, Sr, Ba) and VI (O, S, Se, Te). The combination of several elements of these two groups also gives a multi-component semiconductor [8].

I.6.3. III -V semiconductors

Semiconductors of the III-V family of materials consist of one element in column III and another in column V of the periodic table.

This class of semiconductors finds an important place in the fields of optoelectronics because of their physical and electronic properties such as thermal conductivity, bandgap energy, ... [6].

Boron-based or nitrogen-based compounds belong to the III-V semiconductor family. They are compounds with a large gap, particularly interesting for their applications in the field of high temperatures.

From a crystallographic point of view, III-V semiconductors are known in several crystalline forms.

I.7. Schottky barrier diode

Neville Mott in 1939 and Walter Schottky himself are credited with developing the first-order hypothesis of the creation of a Schottky barrier (SB). Because it does not emphasize the features of the MS interface, the Schottky-Mott theory is frequently broken at a genuine MS interface. Based on the idea of Fermi-level pinning (FLP), a number of models were created to explain the observed deviation of the empirically obtained SBH from the Schottky-Mott relationship. All of these models (gap state models) imply the existence of surface states known as gap states (GS) and an interface specific region (ISR) in the semiconductor's band gap.

The gap state models can be divided into two groups, based on whether the metal and the semiconductor are assumed to interact or not [7].

I.8. Metal semiconductor junction: schottky barrier

The metal-semiconductor junction can result in a junction that has non-linear diode characteristics similar to those of the *p-n* diode except that for many applications it has a much faster response since carrier transport is unipolar. Such a junction is called a Schottky barrier diode. [9]

I.8.1. Schottky Barrier Height

The working of the Schottky diode depends upon how the metal-semiconductor junction behaves in response to external bias. Let us pursue the approximation we used for the *p-n* junction and examine the band profile of a metal and a semiconductor. A metal semiconductor structure is shown in figure I.8a. In figure I.8b and figure I.8c the band profiles of a metal and a semiconductor are shown.

We will assume an ideal surface for the semiconductor in the first calculation. Later we will examine the effect of surface defects. We will assume that $\phi_m > \phi_s$ so that the Fermi level in the metal is at a lower position than in the semiconductor. This condition leads to an *n*−type Schottky barrier. When the junction between the two systems is formed, the Fermi levels should line up at the junction and remain flat in the absence of any current, as shown in figure I.8c. At the junction, the vacuum energy levels of the metal side and semiconductor side must be the same. To ensure the continuity of the vacuum level and align the Fermi levels. Electrons move out from the semiconductor side to the metal side. Note that since the metal side has an enormous electron density, the metal Fermi level or the band profile does not change when a small fraction of electrons are added or taken out. As electrons move to the

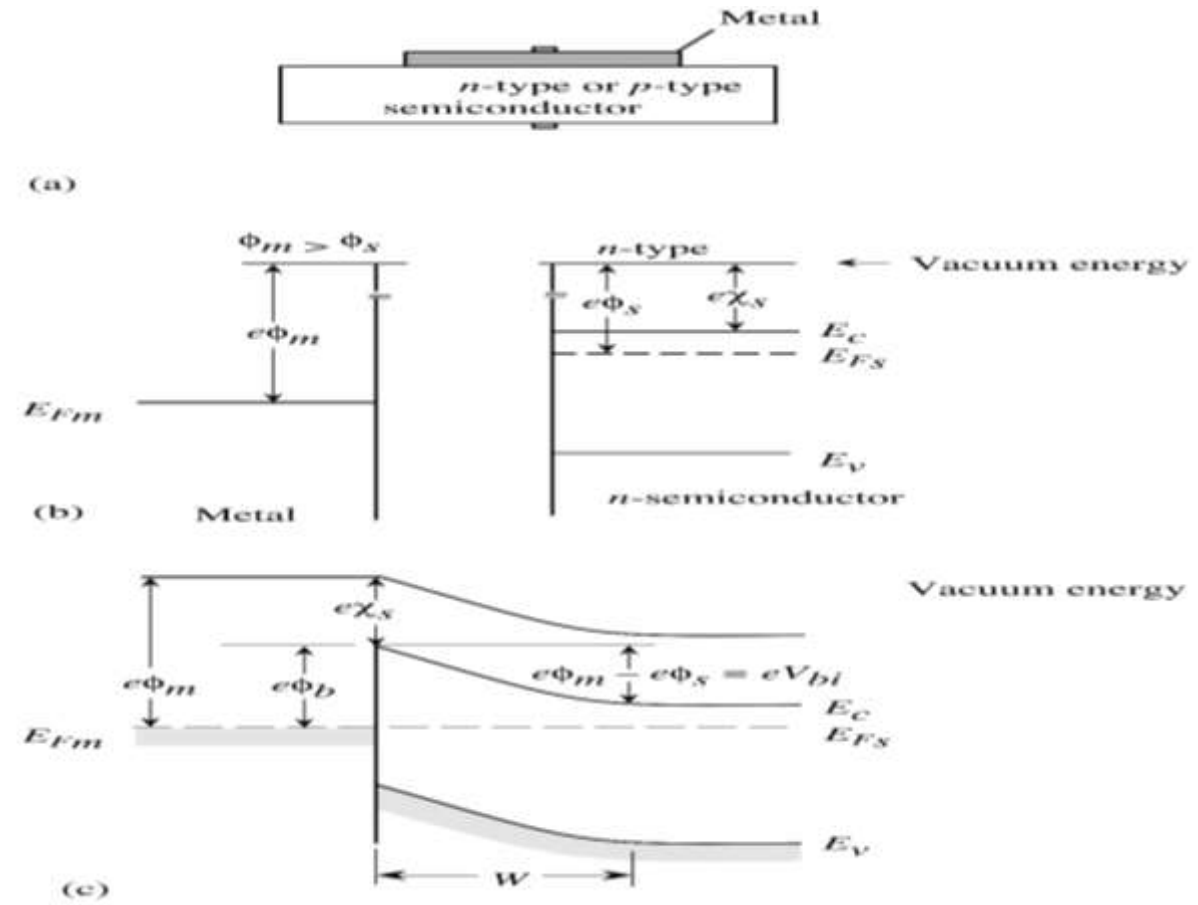
metal side, they leave behind positively charged fixed dopants, and a dipole region is produced in the same way as for the *p-n* diode. [9]

In the ideal Schottky barrier with no bandgap defect levels, the height of the barrier at the semiconductor-metal junction (figure I.8c), is defined as the difference between the semiconductor conduction band at the junction and the metal Fermi level. This barrier is given by (see figure I.8c).

$$e\phi_b = e\phi_m - ex_s \tag{I.1}$$

The electrons coming from the semiconductor into the metal face a barrier denoted by eV_{bi} as shown in figure I.8c. The potential eV_{bi} is called the built-in potential of the junction and is given by

$$eV_{bi} = -(e\phi_m - e\phi_s) \tag{I.2}$$



METAL-SEMICONDUCTOR JUNCTION AT EQUILIBRIUM

Figure I.8: (a) A schematic of a metal-semiconductor junction. (b) The various important energy levels in the metal and the semiconductor with respect to the vacuum level. (c) The junction potential produced when the metal and semiconductor are brought together. Due to the built-in potential at the junction, a depletion region of width W is created.

It is possible to have a barrier for hole transport if $\phi_m < \phi_s$. In figure I.9 we show the case of a metal-p-type semiconductor junction where we choose a metal so that $\phi_m < \phi_s$. In this case, at equilibrium the electrons are injected from the metal to the semiconductor, causing a negative

SCHOTTKY METAL	***n* Si**	***p* Si**	***n* GaAs**
Aluminum, Al	0.7	0.8	
Titanium, Ti	0.5	0.61	
Tungsten, W	0.67		
Gold, Au	0.79	0.25	0.9
Silver, Ag	0.88		
Platinum, Pt	0.86		
PtSi	0.85	0.2	
$NiSi_2$	0.7	0.45	

Table I.1: Schottky barrier heights (in volts) for several metals on n- and p-type semiconductors [9].

and is almost independent of the metal used. The model discussed above provides a qualitative understanding of the Schottky barrier heights. However, the detailed mechanism of the interface state formation and Fermi level pinning is quite complex. In table I.1 we show Schottky barrier heights for some common metal-semiconductor combinations. In some materials such as GaN and AlGaN,the surface retains its ideal behavior and the Schottky barrier is indeed controlled by the metal work function. [9]

Charge on the semiconductor side. The bands are bent once again and a barrier is created for hole transport. The height of the barrier seen by the holes in the semiconductor is

$$eV_{bi} = e\phi_s - e\phi_m \tag{I.3}$$

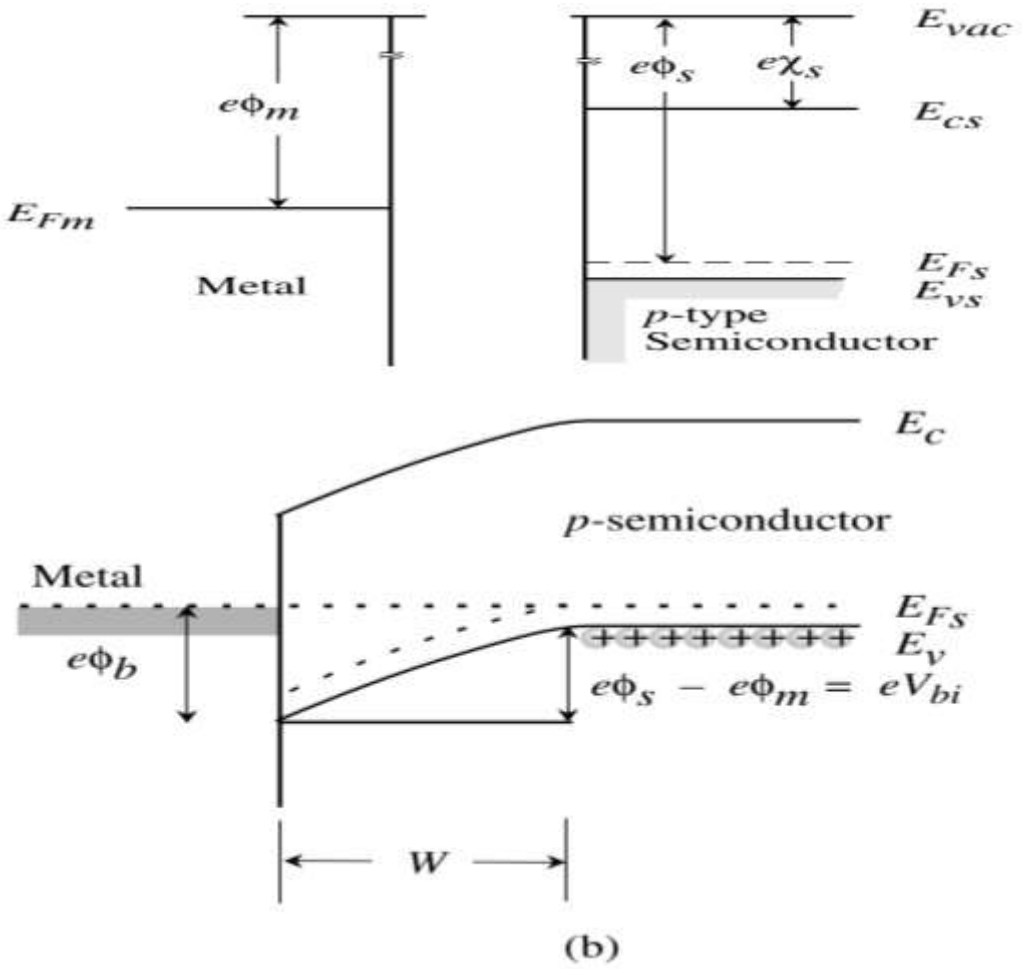


Figure I.9: A schematic of the ideal p-type Schottky barrier formation. (a) The positions of the energy levels in the metal and the semiconductor; (b) the junction potential and the depletion width.

The Schottky barrier height for *n*- or *p*-type semiconductors depends upon the metal and the semiconductor properties. This is true for an ideal case. It is found experimentally that the Schottky barrier height is often independent of the metal employed, as can be seen from table I.1 This can be understood qualitatively in terms of a model based upon non ideal surfaces. In this model the metal-semiconductor interface has a distribution of interface states that may arise from the presence of chemical defects from exposure to air or broken bonds, etc. Surface defects can create $\sim 10^{13}$ cm^{-2} defects if there is 1 in 10 defects at the surface. Surface defects lead to a distribution of electronic levels in the bandgap at the interface, as shown in figure I.10. The distribution may be characterized by a neutral level ϕ_0 having the property that states below it are neutral if filled and above it are neutral if empty. If the density of bandgap states near ϕ_0 is very large, then addition or depletion of electrons to the semiconductor can not alter the Fermi level position at the surface without large changes in surface charges

(beyond the numbers demanded by charge neutrality considerations). Thus, the Fermi level is said to be pinned. In this case, as shown in figure I.10, the Schottky barrier height is

$$e\phi_b = E_g - e\phi_0 \tag{I.4}$$

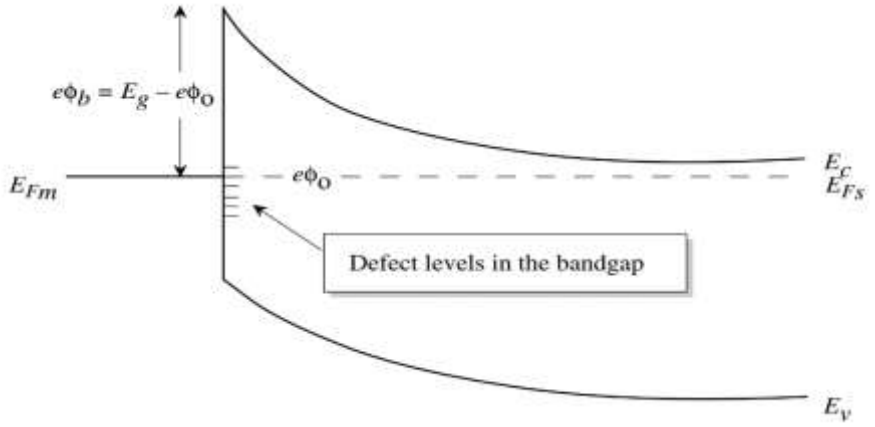


Figure I.10: Interface states at a real metal-semiconductor interface. A neutral level ϕ_0 is defined so that the interface states above ϕ_0 are neutral if they are empty and those below ϕ_0.

I.8.2. Current transport mechanisms in semiconductor contact

The current in the Schottky diode is essentially due to the majority carriers, the transport of current in a metal/semiconductor junction can be done according to the five mechanisms represented in Figure I.11 [9];

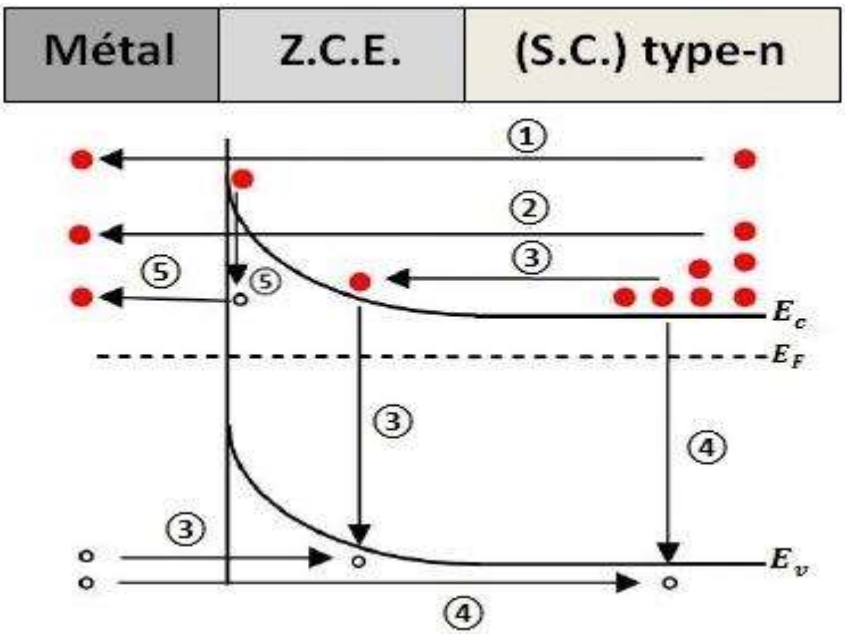


***Figure I.11: Modes of electron transport in a live polarized n-type metal/semiconductor contact* [9]**

1. Passage of electrons with a high energy (called hot electrons) from the semiconductor to the metal over the barrier, two models account for the phenomenon: the thermoionic model (in high-mobility semiconductors) and the diffusion model (in low-mobility semiconductors).
2. Passage of electrons through the barrier by tunneling.
3. Generation-recombination in the ZCE, in direct polarization, this mechanism corresponds to the recombination in the ZCE of an electron coming from the semiconductor with a hole coming from the metal.
4. Injection of minority carriers, in hole metal recombines with an electron of the semiconductor in the quasi-neutral zone of the semiconductor.
5. Recombination current on interface states, the electrons of the semiconductor are trapped at an empty interface center and then they pass through the metal by tunneling.
-When the contact is rectifier, and for weak doping (<1017 cm^{-3}), process (1) is the most important, because it defines the normal functioning of the metal/semiconductor contact, on the other hand mechanisms (2), (3), (4), and (5) cause deviations from the ideal behavior [11].
-The current passes mainly through the barrier by tunneling for strong doping (>1018 cm^{-3}). The contact made is then ohmic.

I.8.3. Polarization of the Schottky diode

I.8.3.1. Direct polarization

When the junction is polarized under a forward voltage V_j, it implies the reduction of the height of the barrier which becomes (V_b-V_j) leading to a decrease in the thickness W:

$$W' = \sqrt{\frac{2\varepsilon}{qN_D}}\left(V_b - V_j\right) \tag{I.5}$$

V_b is replaced by (V_b-V_j), many electrons from the N region and holes from the P region can then cross this potential barrier and, then presenting themselves in a "hostile medium", they are recombined, this recombination consumes near the W depletion region holes in the P region (electrons in the N region), to restore equilibrium, the holes in the neutral region P move towards the zone where recombination occurs (hole deficit), the electrons in the neutral region N are subjected to a similar phenomenon [8].

As the majority carriers continue from the N region to the P region, they become minority where they diffuse and eventually recombine with the majority holes, similarly, the holes permanently generated in the P region will be available to recombine with electrons

crossing the potential barrier, some of the current being produced is due to saturation (IS) and some is due to diffusion (ID).

However, in the direct polarization state the scattering current is much larger than the saturation current see equation (I.4) due to the decrease in the depletion region, Figure (I.12) shows the current–voltage (I-V) characteristic of a Schottky diode in the forward polarization state.

$$I_{Total} = I_S - I_D \approx I_D \tag{I.6}$$

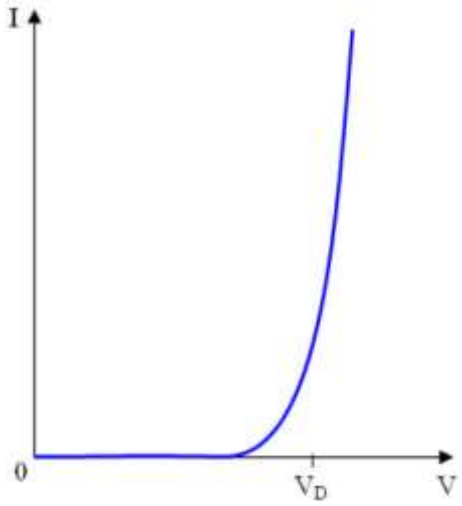


Figure I.12: Current-voltage characteristic of a direct-biased Schottky diode.

I.8.3.2. Reverse polarization

If the junction is polarized in the opposite direction, the potential barrier height between the P and N regions is reinforced by the applied inverse external voltage (V_{inv}) and becomes (V_b+V_{inv}).

The electric field in the space charge region increases as well as its thickness W (in equation (I.7), V_b becomes (V_b+V_{inv}). The majority carriers of the N and P a regions do not have the energy to jump this potential barrier. The junction is then crossed by a very low saturation current I_S [10].

In case of reverse polarization, the probability that an electron will have enough energy to overcome the potential barrier is very low and the junction will act as an insulator, not allowing current to flow, with the growth of the depletion region, the scattering current (I_D) is very low and the total current in the system is approximately equal to the saturation current (I_S) as shown in the following equation:

$$I_{Total} = I_S + I_D \approx I_s \tag{I.7}$$

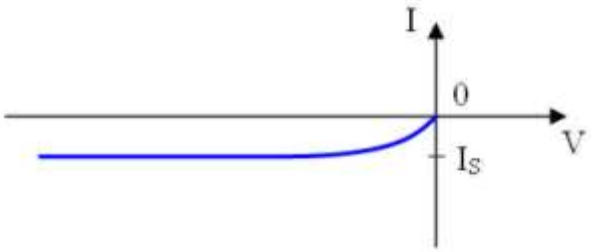


Figure I.13: Current-voltage characteristic of a reverse-polarized Schottky diode.

I.8.4. Applications of Schottky diodes

The efficiency of these diodes determines the choice of their applications, they are widely used in radio mixers and radio frequency detectors, they meet the requirements of these applications thanks to their capabilities of operation at very high frequencies in the MHz range.

Schottky diodes are also used to protect transistors through a process called voltage blocking, this role is made possible by their low voltage drop. Diodes are often used as a kind of reference or limit, they allow flow in one direction, but block it in the other direction, this way of working makes them very useful for protecting sensitive devices from currents flowing in the opposite direction.

If a battery or battery bank is recharged by an external power source, the current must flow in one direction to recharge them, without its direction of flow ever being reversed, since this would drain the battery(ies), Schottky diodes are commonly used for this specific application, switching power systems also use these devices to control the flow of current. Such systems power many types of devices, including computers [12].

I.8.5. The advantages of the Schottky diode

The advantages of the Schottky diode can be found in the following points [13]:

- The low junction capacitance allows this type of diode to be used in very high frequency (RF) applications.
- The Schottky diode can operate at frequencies of the order of 20GHz.
- The junction potential, for a given current, is lower than that of conventional diodes and the recovery time is very short (10 ns) even for high currents.
- Low noise figure.
- Low energy dissipation.

I.9.Silicon, structure and properties

Semiconductors are the materials used in the manufacture of electronic and optoelectronic devices. Among the various types of the latter, silicon. Although very old, it is still widely used today thanks to its semiconductor properties and its ability to withstand extreme environments in terms of pressure, temperature and dissipated power. In fact, silicon is the basic material of 90% of the microelectronics industry, it is found in the manufacture of diodes, transistors, increasingly efficient integrated circuits and photovoltaic panels. [7]

Silicon was discovered in 1824 by J.J. BERZELIUS in Stockholm, Sweden. It is, after carbon, the most abundant element on earth. It is obtained by reducing silica by carbon. [8]

$$SiO_2 + 2C \rightarrow Si + CO_2 \quad \text{(I.8)}$$

Silicon is a covalent crystal of Column IV. The four peripheral electrons are pooled with four neighbors and establish valence bonds and the properties of the crystals will depend on the strength of these bonds.

I.9.1 Silicon types

Like many other elements, silicon can exist at room temperature under different structures, the two most common of which are the amorphous state and the crystalline state (monocrystalline or multicrystalline) respectively.

a. Monocrystalline silicon

The monocrystalline structure is de... denies as being an orderly and periodic arrangement of atoms within a crystallographic lattice whose elementary element is called a lattice. The crystalline silicon in the diamond structure, which is a combination of two interpenetrated face-centered cubic structures (CFCs), with an interatomic distance or lattice parameter d = 2:35A°. Monocrystalline technology uses silicon lingo that is also used in the manufacture of several electronic devices. Monocrystalline silicon is a raw material of very high purity, a monocrystalline silicon wafer is composed of a single grain.

b. Amorphous silicon

Amorphous silicon has a disordered, non-crystallized, glassy atomic structure, but it has a light-absorbing coefficient about 1000 times greater than crystalline silicon. However, the high defect density of amorphous silicon (dangling bonds, interface states, multisristalline structure) limits its conversion efficiency, which is less than 10% for electronic devices such as industrialized solar cells. [9]

I.9.2. Atomic structure

Figure I.14 illustrates the difference in the atomic structure between single crystal silicon and a-Si:H. Figure I.14(a) shows the structure of single crystal silicon schematically. Each Si atom is covalently bonded to four neighboring Si atoms. All bonds have the same length and the angles between the bonds are equal. The number of bonds that an atom has with its immediate neighbors in the atomic structure is called the coordination number or coordination. Thus, in single crystal silicon, the coordination number for all Si atoms is four; we can also say that Si atoms are fourfold coordinated. A unit cell can be defined, from which the crystal lattice can be reproduced by duplicating the unit cell and stacking the duplicates next to each other. Such a regular atomic arrangement is described as a structure with long range order. A diamond lattice unit cell represents the real lattice structure of single crystal silicon [14].

Figure I.14(b) illustrates that a-Si:H does not exhibit the structural order over a long range as is the case for single crystal silicon. Nevertheless, there is a similarity in atomic configuration on a local atomic scale, where most Si atoms have covalent bonds with four neighbors. The a-Si:H has the same short-range order as the single crystal silicon but it lacks the long range order. The small deviations in bonding angles and bonding lengths between the neighboring atoms in a-Si:H lead to a complete loss of the locally ordered structure on a scale exceeding a few atomic distances. The resulting atomic structure of a-Si:H is called the continuous random network. Due to the short-range order in the continuous random network of a-Si:H, the common semiconductor concept of the energy states bands, represented by the conduction and valence bands, can still be used [14].

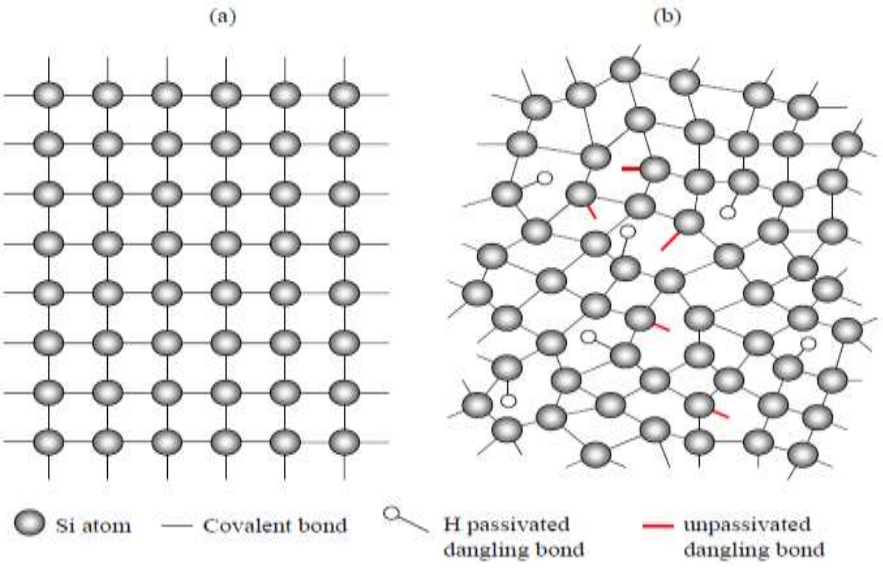


Figure I.14: Schematic representation of the atomic structure of (a) single crystal silicon, (b) hydrogenated amorphous silicon.

The larger deviations in bonding angles and bonding lengths between the neighboring atoms in a-Si:H result in the so-called weak or strained bonds. The energy of the weak bonds is higher than the energy of optimal silicon covalent bonds in ideal single crystal silicon. Therefore, the weak bonds can easily break and form defects in the atomic network. We note that in the continuous random network, the definition of a defect is modified with respect to the crystal structure. In a crystal any atom that is out of place in a lattice forms a defect. In the continuous random network an atom cannot be out of place. Because the only specific structural feature of an atom in the continuous random network is the coordination to its neighbors, a defect in a-Si:H is the coordination defect [14].

This happens when an atom has too many or too few bonds. In a-Si:H the defects are mainly represented by Si atoms that are covalently bonded to only three Si atoms (threefold coordinated) and have one unpaired electron, a so-called dangling bond. Since this configuration is the dominant defect in a-Si:H, the defects in a-Si:H are often related to the dangling bonds.

When amorphous silicon is deposited in such a way that hydrogen can be incorporated in the network (as in the case of glow discharge deposition from silane), then the hydrogen atoms bond with most of the dangling bonds. We say that the dangling bonds are passivated by hydrogen. Hydrogen passivation reduces the dangling bond density from about 10^{21} cm^{-3} in pure a-Si (amorphous silicon that contains no hydrogen) to 10^{15}-10^{16} cm-3 in a-Si:H, i.e. less than one dangling bond per million Si atoms. In Fig. 1.6(b) some of the defects with unpassivated dangling bonds and with hydrogen passivated dangling bonds are depicted. Device quality a-Si:H contains from 1 to 10 atomic percent of hydrogen. In summary, the short range order in a-Si:H network and the hydrogen passivation of the dangling bonds are responsible for semiconductor properties of amorphous silicon [14].

I.9.3. Density of energy state

The difference in the atomic structure between single crystal silicon and a-Si:H leads to the different distributions of density of allowed energy states as schematically illustrated in Figure I.15. The periodic atomic structure of single crystal silicon results in the ranges of allowed energy states for electrons that are called energy bands and the excluded energy ranges, forbidden gaps or band gaps. Figure I.15 (a) shows schematically the distribution of density of states for single crystal silicon, in which the valence band and the conduction band are separated by a well-defined band gap, Eg. At room temperature single crystal silicon has a band gap of 1.12 eV. In case of an ideal crystal, there are no allowed energy states in the band gap [14].

As Figure I.15 (b) demonstrates, in case of a-Si:H, there is a continuous distribution of density of states and no well-defined band gap exists between the valence band and the conduction band. Due to the long range order disorder in the atomic structure of a-Si:H the energy states of the valence band and the conduction bands spread into the band gap and form regions that are called band tail states. The band tail states represent the energy states of electrons that form the strained bonds in the a-Si:H network. The width of the band tails is a measure for the amount of disorder in a-Si:H material. More disorder in a-Si:H means that the band tails are broader. In addition, the dangling bonds introduce allowed energy states that are located in the central region between the valence band and conduction band states [14].

The electron and hole wave functions that extend over the whole structure are characteristic for energy states, in which the charge carriers can be considered as free carriers. These states are non-localized and are called extended states. The wave functions of the tail and defect states are localized within the structure and therefore these states are called localized states. Consequently, mobility that characterizes transport of carriers through the localized states is strongly reduced. This feature of a sharp drop of mobility of carriers in the localized states in a-Si:H is used to define its band gap. This band gap is denoted by the term mobility gap, E_{mob}, because the presence of a considerable density of states in this gap conflicts the classical concept of the band gap. The energy levels that separate the extended states from the localised states in a-Si:H are called the valence band and the conduction band mobility edges.

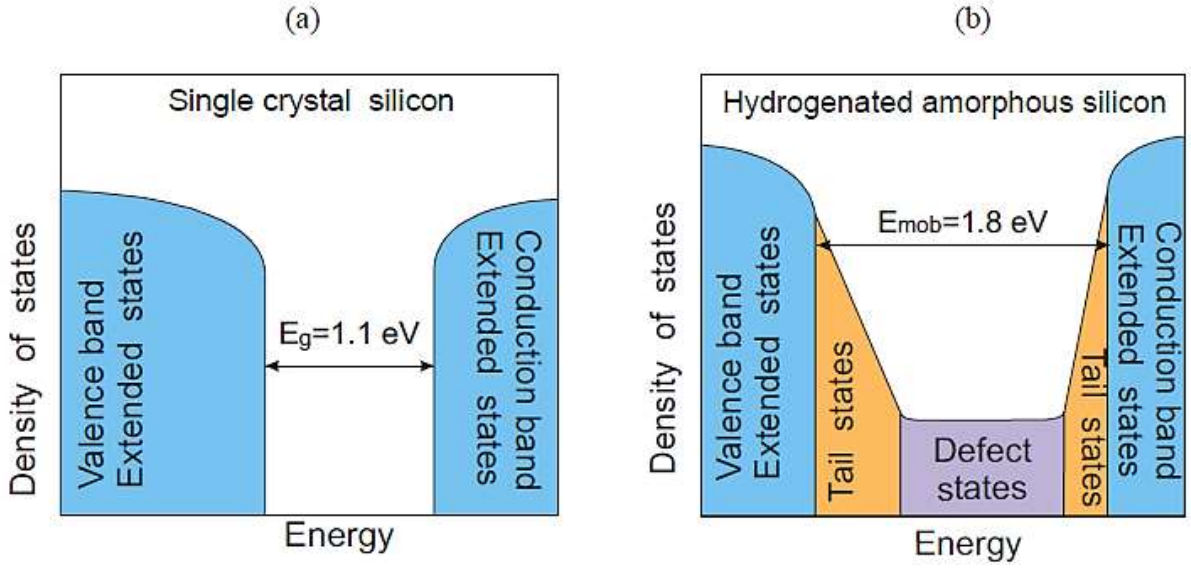


Figure I.15: The schematic representation of the distribution of density of allowed energy states for electrons for (a) single crystal silicon (b) a-Si:H.

The mobility gap of a-Si:H is larger than the band gap of single crystal silicon and has a typical value of 1.8 eV. The localised tail and dangling bond states have a large effect on the electronic properties of a-Si:H. The tail states act as trapping centres and build up a space charge in a device, the dangling bond states act as very effective recombination centres and affect in particular the lifetime of the charge carries [14].

I.9.4 Electrical properties

Owing to the differing arrangement of Si and C atoms within the SiC crystal lattice, each SiC polytype exhibits unique fundamental electrical and optical properties. Some of the more important electrical properties of the 3C-, 4H-, and 6H-SiC polytypes are given in Table (I.2) [15]. Even within a given polytype, some important electrical properties are non-isotropic, in that they strongly depend on the crystallographic direction of the current flow and the applied electric field (for example, electron mobility for 6H-SiC). [16]

	Si	**4H-SiC**	**6H-SiC**	**3C-SiC**
Bandgap energy Eg [eV]	1.12	3.26	3.03	2.4
Relative dielectric constant ε_s	11.9	9.7	9.66	9.72
Breakdown Field E_B @ $N_D = 10^{17}\ cm^{-3}$ [MV/cm]	0.3	$\parallel$ c-axis: 3.0	$\parallel$ c-axis: 3.2 $\perp$ c-axis: >1	> 1.5
Thermal Conductivity κ [W/cmK]	1.31	4.9	4.9	3.2
Intrinsic Carrier Concentration n **[**cm^{-3}**]**	$9.65 * 10^{9}$	$5 * 10^{-9}$	$1.6 * 10^{-6}$	$1.5 * 10^{-6}$
Electron Mobility μ_n @ $N_D = 10^{16}\ cm^{-3}$ [cm^2/Vs]	1430	$\parallel$ c-axis: 900 $\perp$ c-axis: 800	$\parallel$ c-axis: 60 $\perp$ c-axis: 400	800
Hole Mobility μ_p	480	115	90	40

@ $N_A = 10^{16}$ cm^{-3} [cm^2/Vs]				
Saturated Electron Velocity v [10^7 cm/s]	1	2	2	2.5
Donors & Ionization Energy ΔE_d[meV]	P: 45 As: 54	N: 50, 92 P: 54, 93	N: 85, 140 P: 80, 110	N: 50
Acceptors & Ionization Energy ΔE_a[meV]	B: 45 Al: 67	Al: 200 B: 285	Al: 240 B: 300	Al: 270
2003 Commercial Wafer Diameter [inches]	12	3	3	?

Table I.2: Comparison of electrical properties of SiC polytypes with Si 16]

I.9.5. Silicon Surface

- **Oxidized surface**

Unless very special precautions are used, the surface of silicon is always covered by a layer of natural oxide [17], of thin thickness (a few Angstroms to a few tens of Angstroms), which has a preponderant influence on the behavior of the space charge zone of the semiconductor. Despite this, very little research has been devoted to the study of this oxide; on the other hand, many studies have aimed to specify the characteristics of thick SiO2 layers (a few hundred Angstroms) because of their importance in the semiconductor device industry. However, the properties of these oxides depend essentially on those of the interface and it can be assumed that in reality they are quite similar, whether the oxide is natural or voluntarily deposited. [17]

- **Surface states:** These are electronic states that exist at the surface due to the disruption of the periodic crystal structure. They lie within the silicon bandgap and can trap charge carriers, affecting recombination and electrical characteristics.
- **Surface charge**: Depending on chemical treatments, oxidation, or doping, the surface may carry a net positive or negative charge. This causes band bending, which modifies the electrical potential near the surface.

- **Interface properties:** Especially at the Si/SiO_2 interface (critical in MOSFETs), the density of interface traps and fixed oxide charges influences threshold voltage, leakage, and overall device performance.
- **Passivation:** Techniques like hydrogen passivation are used to neutralize dangling bonds and reduce the density of surface states, improving electrical behavior.

I.10. Conclusion

The basic characteristics of semiconductors were examined in this chapter, along with their crystal structures and the ways in which they vary from metals and insulators in their conduction mechanisms. Free electrons allow metals to conduct electricity, whereas semiconductors have conditional conductivity and insulators do not. We made a distinction between extrinsic semiconductors, which are improved by doping to produce n-type or p-type materials, and intrinsic semiconductors, which depend on thermal excitation.

Then we gave a detailed description of the Schotki diode, the components and structure of which we showed, in addition, the different polarization conditions of the Schotki diode and its characteristics were well clarified, and finally, its applications in various fields and its advantages were described.

Chapter II

Techniques for extracting Schottky diode parameters

II.1. Introduction

Schottky diodes are vital electronic components widely used in high-frequency applications, microelectronics, solar energy systems, and fast power rectification, thanks to their distinctive features such as low forward voltage drop and high switching speed. To understand their performance and optimize their integration into electronic circuits, it is essential to accurately determine a set of key parameters, including the barrier height (Φ_B), ideality factor (n), reverse saturation current (I₀), and series resistance (R_s).

Several analytical and mathematical techniques are available to extract these parameters from current–voltage (I–V) or capacitance–voltage (C–V) characteristics. These include the Shockley model, Cheung's method, Norde's technique, and more advanced numerical fitting approaches. The main goal of these techniques is to provide an accurate representation of the diode's real behavior, thereby enhancing the overall performance of systems that rely on Schottky diodes. [27].

II.2. Current-voltage methods

II.2.1. Standard method

The hypotheses of this method are:

- $\emptyset_{b0}$ is determined from the saturation equation even if $n \geq 1$
- $\emptyset_{b0}$ and n are voltage independent
- equation for $V_d = V - R_S \gg nkT/q$, and becomes:

$$I = I_s exp\left(\frac{q(V - R_S I)}{nkT}\right) \tag{II.1}$$

By deriving equation (II.1) as function to the voltage V, the ideality fact can be expressed as

$$n = \frac{q}{kT}\frac{dV}{dln(I)} \tag{II.2}$$

Where $dV/d[Ln(I)]$ is the slope of region 2 in figure (II.1). The plot of $Ln(I)_{VS.}\ V$ remain a straight line as long as $V \gg nkT/q$ and $V \gg R_S I$.

The zero bias BH $\emptyset_{b0}$ can be calculated by rewriting the saturation current Equation as

$$\emptyset_{b0} = \frac{kT}{q} ln\left(\frac{AA^* T^2}{I_s}\right) \tag{II.3}$$

The saturation current I_s is derived from the straight line intercept of $Ln(I)\ at\ V = 0$ as shown in figure (II.1).

This method is especially limited by the value of the series resistance, i.e. for high series resistance the region 2 shrinks and shows no linear regime. Another problem arises when thermionic current is not the dominant transport mechanism, in this case $\emptyset_{b0}$ determined from equation (II.3) is only the result of calculation and has no real physical meaning [28]

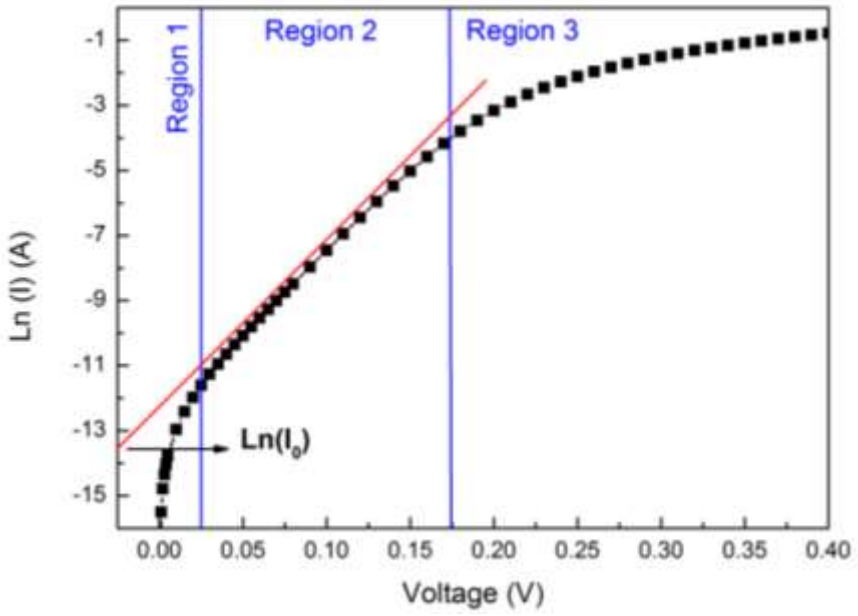


Figure II.1: Typical I-V characteristic of Schottky diode [28].

II.2.2. Norde method

According to Norde [29] the problem with a series resistance can in many cases be avoided by using a plot of the function

$$F(V) = \frac{V}{2} - \frac{kT}{q} ln\left(\frac{I(V)}{AA^{*}T^{2}}\right) \tag{II.4}$$

Equation (II.4) and equation (II.1) will give

$$F(V) = \emptyset_{b0} + IR_S - \frac{V}{2} \tag{II.5}$$

From equation (II.4), by plotting $F(V)$ as function of the voltage, the plot will be a straight line with negative slope ($F(V)$ decreases) in the bias range where the series resistance is neglected. Then $F(V)$ will start to increase as straight line in the bias range where the series resistance is dominated. The minimum of the $F(V)$ plot is the point of interest.

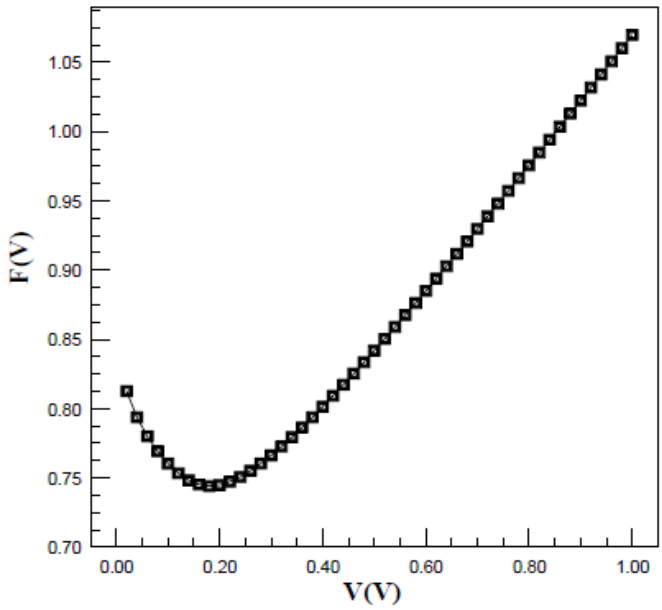


Figure II.2: Example of F(V) vs. V plot from [30]

After some mathematical calculation, Norde derived $\emptyset_{b0}$ and R_S as function of $F(V_{min})$ which is the minimum of $F(V)$ plot, $Vmin$ which is the corresponding voltage to $F(V_{min})$ in $F(V)$ plot and I_{min} which is the current corresponding to V_{min} in the I-V characteristic.

$$\emptyset_{b0} = F(V_{min}) + \frac{V_{min}}{2} - \frac{kT}{q} \tag{II.6}$$

$$IR_S = \frac{kT}{qI_{min}} \tag{II.7}$$

The Norde method was originally assumed the ideality factor n to be unity, thus for non-ideal diodes ($n > 1$) the series resistance is given by the expression [30-31]

$$R_S = \frac{(2-n)kT}{qI_{min}} \tag{II.8}$$

II.2.3 Cheung method

S. K. Cheung and N. W. Cheung in [32] proposed an alternate approach to determine the series resistance, the ideality factor and the zero bias BH from the I-V data using two plots. equation (II.1) can be rewritten in term

$$V = R_S I + n\emptyset_{b0} + \frac{n}{\beta} ln\left(\frac{I}{AA^* T^2}\right) \tag{II.9}$$

Differentiating equation (II.9) with respect to I and rearranging terms, the next equation can be obtained

$$\frac{dV}{dLn(I)} = R_S I + \frac{n}{\beta} \tag{II.10}$$

By plotting dV/dLn (I) vs. I a straight line will be obtained as shown in figure (II.3). From equation (II.10), R_S = slop and n/β = $\text{intercept}_{\text{Y.axis.}}$

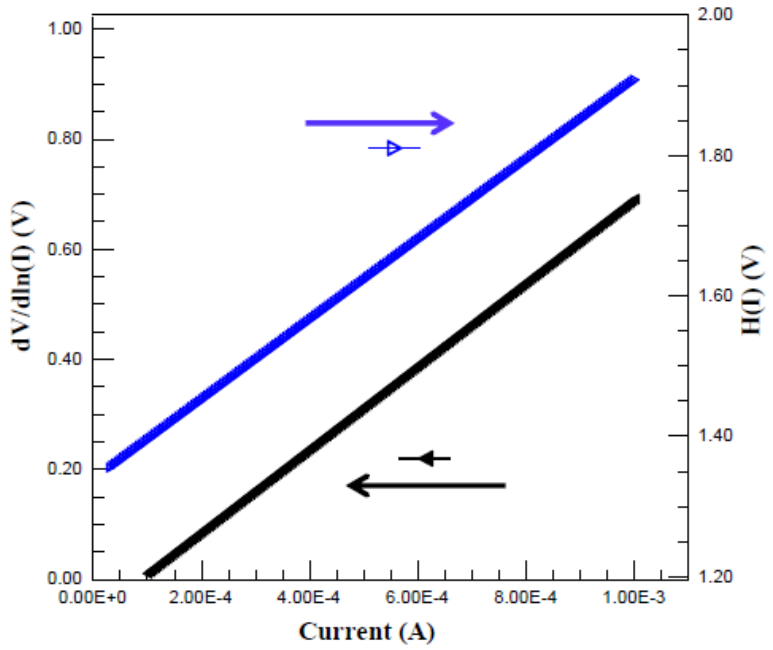


Figure II.3: Example of dV/d(lnI) vs. I and H(I) vs. I plots from [30]

To evaluate $\emptyset_{b0}$, the authors define the function H(I):

$$H(I) = V - \frac{n}{\beta} ln\left(\frac{I}{AA^{*}T^{2}}\right) \tag{II.11}$$

From equation (II.9)

$$H(I) = R_S I + n\emptyset_{b0} \tag{II.12}$$

Using equation (II.11) and the value of n determined from the previous plot the value of H(I) can be calculated. By plotting H(I) vs. I a straight line will be obtained as shown in figure (II.3). From equation (II.12), $n\emptyset_{b0}$ = $\text{intercept}_{\text{ordinate}}$, the slope of this plot also provides a second determination of RS which can be used to check the consistency of this approach.

II.3. Flat-band barrier height

A basic BH defined at zero electric field, the flat-band BH ($\emptyset fb$) offers a more accurate description of the physical barrier at the MS junction. Since there is no charge in the surface states at zero electric field, the shift of the BH is zero. Furthermore, because the semiconductor bands are flat, the properties cannot be impacted by tunneling or image force reduction. The zero-bias BH and ideality from an I-V measurement are related by the flat-band barrier height, which is determined by [33]

$$\emptyset_{fb} = Vn\emptyset_{b0} - (n-1) - \frac{kT}{q} ln \frac{N_C}{N_D} \quad \text{(II.13)}$$

If the flat band condition is certainly occurred and the extracted ideality value are correct, $\emptyset_{fb}$ should be constant. It appears that $\emptyset_{fb}$ is a fundamental BH and provides a better characterization of the physical barrier at the MS junction compared with $\emptyset_{b0}$.

If the flat band condition is certainly occurred and the extracted ideality value are correct, $\emptyset_{fb}$ should be constant. It appears that $\emptyset_{fb}$ is a fundamental BH and provides a better characterization of the physical barrier at the MS junction compared with $\emptyset_{b0}$.

II.4. Activation energy measurement

The main benefit of determining SBH via an activation energy measurement is that, unlike previous approaches, no electrically active area assumption is needed. Because the active area may not always be recognized or may be greater or less than the expected size [34]. The Richardson plot, which plots Ln (I_S / T^2) vs. 1/T, serves as the basis for the activation energy measurement.

Richardson plot can be obtained by rewriting the saturation current equation as

$$Ln\left(\frac{I_s}{T^2}\right) = Ln(AA^*) - \frac{q\emptyset_{b0}}{kT} \quad \text{(II.14)}$$

The figure should be linear, with the slope giving the activation energy, which is $\emptyset_{b0}$ ($-q\emptyset_{b0}/k$ = slope), and the ordinate intercept at $10^3/T = 0$ giving the Richardson constant for a given diode area ($Ln(AA^*)$ = intercept). The BH Richardson constant for a non-ideal Schottky diode with a temperature-dependent value will be far from the theoretical value. Furthermore, as seen in figure (II.4), the Richardson plot of the majority of experimental investigations deviates from linearity at low temperatures; in this instance, the linear fitting of the linear area determines the slope and the intercept. As mentioned in the previous chapter, the variation of

the BH was interpreted in the experimental studies by BH in homogeneities based on Werner and Guttler model or Tung model. As a result, the Richardson plot is typically modified or corrected using the two models. The bowing of the Richardson plot and the difference between the theoretical and obtained value of the Richardson constant are caused by the BH dependence on temperature.

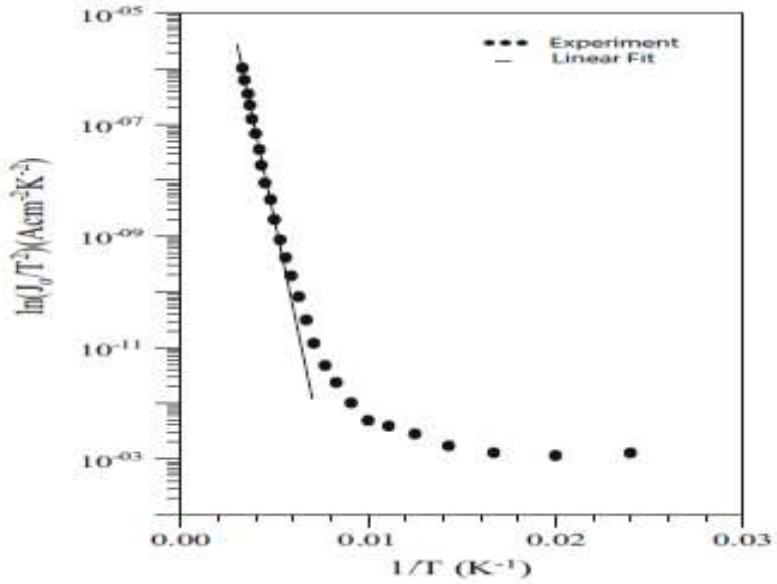


Figure II.4: Example of Richardson plot from [35]

II.4.1. Modified Richardson plot with Werner and Guttler model

The modified Richardson plot relation is obtained by rewriting the saturation current equation from Werner and Guttler model [20-23]

$$Ln\left(\frac{I_s}{T^2}\right) - \left(\frac{q^2\sigma_0^2}{2k^2T^2}\right) = Ln(AA^*) - \frac{q\overline{\emptyset}_{b0}}{kT} \qquad \text{(II.15)}$$

The values of σ_0 are obtained from the plot of $\emptyset_{b0}$ vs. 1/2kT (figure II.5). The plot should be a straight line where the intercept at ordinate gives the mean barrier $\overline{\emptyset}_{b0}$ ($\overline{\emptyset}_{b0}$= intercept) and the slop gives the standard deviation of the Gaussian distribution of the BH ($-\sigma_0^2$= slope). If the plot is mot linear in some temperature range, the model should not be used to interpret the data in that temperature range.

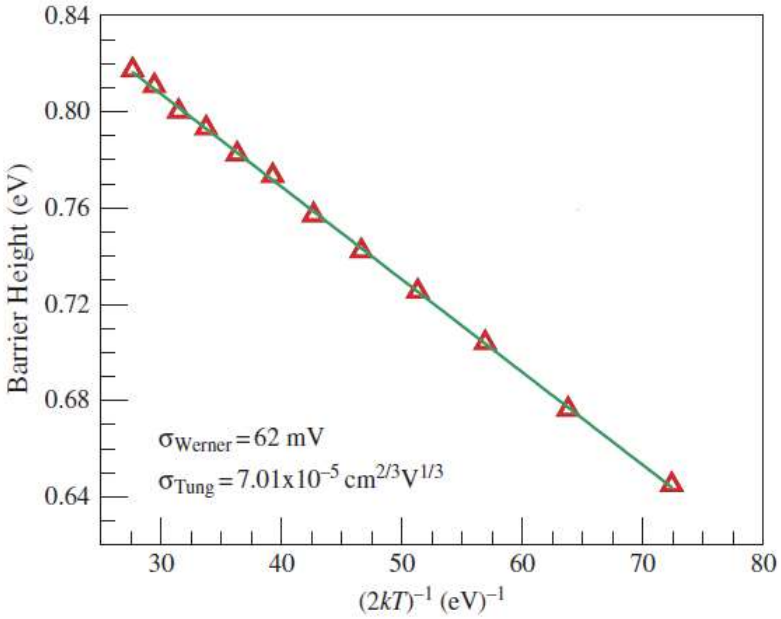


Figure II.5: Example of Øb0 vs. 1/2kT plot from [36]

As shown in figure (II.6) the modified Richardson plot has a straight line where the intercept at ordinate yields A^* ($Ln(AA^*)$ = intercept) and the slop yields the mean barrier $\overline{\emptyset}_{b0}$ ($-q\overline{\emptyset}_{b0}/k$ = slope). When A^* and $\overline{\emptyset}_{b0}$found in good agreement with the theoretical A^* and $\overline{\emptyset}_{b0}$ from $\emptyset_{b0}$ vs. 1/2kT plot respectively, the diode parameter temperature dependence explained based on BH Gaussian distribution of Werner and Guttler model [20-23]. The disadvantages of this modified Richardson plot are: σ_0 should be taken from the plot of $\emptyset_{b0}^c - \emptyset_{b0}$ vs. 1/2kT not from $\emptyset_{b0}$ vs. 1/2kT plot. Secondly $\overline{\emptyset}_{b0}$ taken from modified Richardson plot should be compared with $\emptyset_{b0}^c$ not with $\overline{\emptyset}_{b0}$ from $\emptyset_{b0}$ vs. 1/2kT plot. Finally, the area used to calculate A^* from the intercept is the area of the entire contact not the area of the small regions with low BH.

II.4.2. Modified Richardson plot with Tung model

From the total current equation of Tung model equation, we can write the saturation current of patches as

$$I_s = A_{eff}A^*T^2 exp\left[-\beta\left(\emptyset_{b0} - \frac{\sigma_1^2}{2kT}\left(\frac{V_{bb}}{\eta}\right)^{2/3}\right)\right] \quad \text{(II.16)}$$

The modified Richardson plot relation can be obtained by rewriting equation (II.16) [35-37]

$$Ln\left(\frac{I_s}{A_{eff}T^2}\right) - \frac{\sigma_1^2 {V_{bb}}^{2/3}}{2k^2T^2\eta^{2/3}} = Ln(A^*) - \frac{q\emptyset_{b0}}{kT} \quad \text{(II.17)}$$

The values of σ_1^2 are obtained from the plot of $\emptyset_{b0}$ vs. 1/2kT (figure. II.5). the intercept at ordinate gives the homogeneous barrier $\emptyset_{b0}$ ($\emptyset_{b0}$ = ntercept) and the slop gives the standard deviation σ_1^2 of the patch parameter γ ($-\sigma_1^2\left(\frac{V_{bb}}{\eta}\right)^{2/3}$ = slope). $A_{eff} = AC_1A_p$, the area of the entire Schottky contact A is known. The effective area of one patch A_p can be determined at each temperature. The value of the patches density C_1 must be adjusted until the intercept modified Richardson plot (figure.II.6) gives a Richardson constant value in good agreement with the theoretical value (Ln(A*)=intercept). The slop yields the homogenous barrier $\emptyset_{b0}$($-q\emptyset_{b0}/k$ = slope), $\emptyset_{b0}$ also must be in good agreement with $\emptyset_{b0}$ determined from $\emptyset_{b0}$ vs. 1/2kT plot.

In literature, the value of $C1$ was found in [33, 26] for Schottky contact based on n-InP between (5.85×10^6 and 2.5×10^{10} cm^{-2}), for Schottky contact based on n-GaAs between (3.6×10^7 and 1.2×10^{12} cm^{-2}) in [35, 24] and between (2×10^8 and $5.5\times10^9 cm^{-2}$) for Schottky contact based on 4H-SiC in [28, 37]

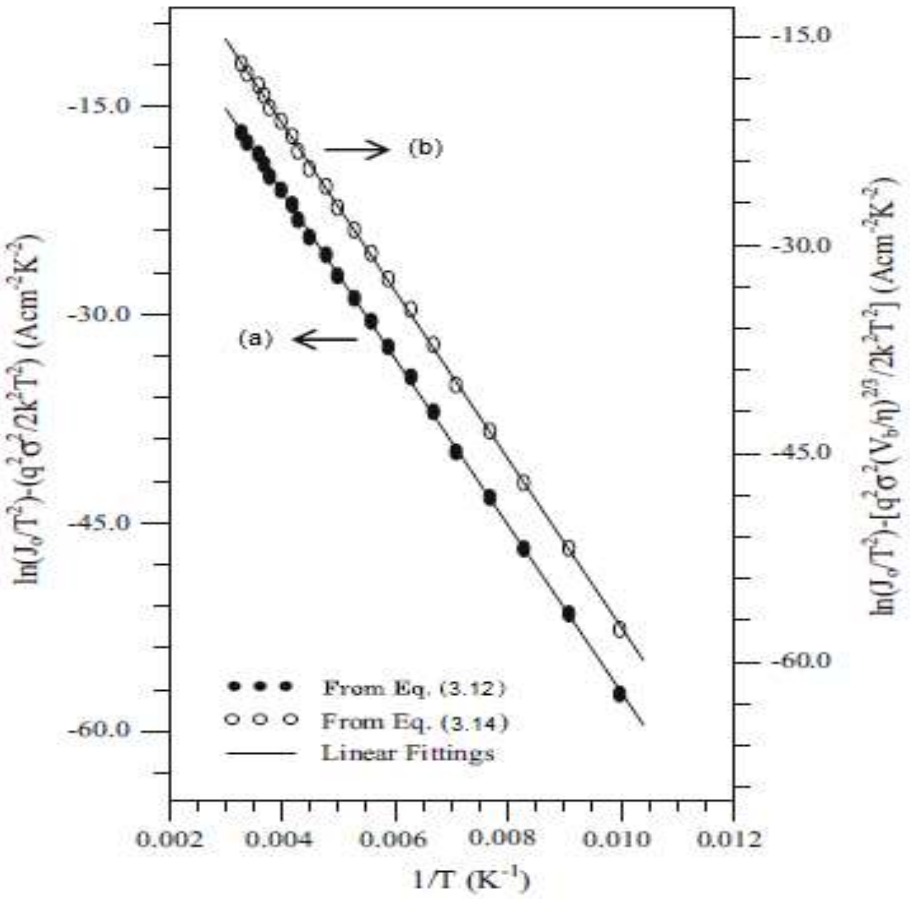


Figure II.6: Example of modified Richardson plot with: (a) Werner and Gutller model, (b)Tung model, from [35].

II.5. Conclusion

This section reviewed key techniques for extracting Schottky diode parameters based on current–voltage (I–V) characteristics. The standard method provides a basic foundation, while advanced approaches like the Norde and Cheung methods offer improved accuracy in determining parameters such as ideality factor and series resistance.

The concept of flat-band barrier height was highlighted as a more accurate representation of the true barrier, especially in non-ideal junctions. Additionally, the modified Richardson plots, using the Werner–Guttler and Tung models, were introduced to account for barrier inhomogeneities in activation energy measurements.

Together, these methods enable a deeper understanding of Schottky diode behavior, supporting the development of more efficient electronic devices.

Chapter III

Simulation and Results

III.1. Introduction

The operation of the Schottky diode is generally described by the current-voltage (I-V) characteristic, which provides information on the mechanisms of internal electrical transport and on the imperfections in the technological steps during the manufacturing process. This characteristic depends on several electrical parameters, such as the series resistance Rs, the barrier height ΦB, and the ideality factor n. Numerous studies have focused on the extraction of these parameters. The accurate determination and knowledge of these parameters allow for a better understanding and explanation of certain electrical phenomena in these junctions.

In this chapter, we present, on one hand, our simulation work on the current-voltage (I-V) electrical characteristics under forward and reverse bias for MS and MIS structures. On the other hand, the extraction techniques for the main parameters mentioned above are developed, namely the Standard (I-V) method and the Cheung's methods.

We will use the Atlas-Silvaco simulator to study and simulate the Schottky diode. First, we show the structure of the Schottky diode with its different regions and their doping profiles. Then, we present the various parameters used in the simulation. Finally, the simulation results of the Schottky structure will be presented, and the effect of temperature on the characteristics of the Schottky diode will be discussed in order to describe the behavior of these diodes for high-temperature applications.

III.2. High temperatures I-V characteristics

We must identify the phenomenon causing the temperature dependency of the Schottky diode parameters since we thought that the BH inhomogeneity had no effect on the I-V characteristics. In order to determine the ideal I-V-T characteristics, we decided to start with the ideal scenario. This provides us a sense of the physical models that have to be employed in order to regenerate the experimental I-V-T characteristics.

III.3. Parameter extraction

The obtained values of the Schottky barrier height and the ideality factor as a function of temperature are shown in table.III.3. As can be seen, the n values deviate from unity and shows a temperature dependence (increase with standard method and decrease with Cheung's method), such a behavior can be attributed to the voltage drop across the large series resistance.

As it is well known the ideality factor is obtained from the linear region before the region where he curves is strongly affected by the voltage drop across the series resistance. This linear region shrinks and shows more nonlinear regime with increasing temperature due

to the increase of the series resistance. On the other hand, the $\emptyset IV$ values are temperature independent and shows a good agreement between the three methods.

III.3.1. MIS

Table III.1 displays the extracted values of the ideality factor (n) and Schottky barrier height (ϕb0) for a near-ideal Metal-Insulator-Semiconductor (MIS) diode at room temperature (300 K). These values are obtained using three common extraction techniques: Standard, Norde, and Chung, allowing a comparative analysis of each method's reliability when applied to MIS structures.

Table III.1: The extracted n and $\emptyset b0$ values of the near ideal diode MIS

Temp (K)	**n**		**$\emptyset b0$ (eV)**		
	standard	**chung**	**standard**	**Norde**	**chung**
300	2.42684	14.85	0.81888	0.83615	0.58

Table III.1 presents the extracted ideality factor (n) and Schottky barrier height (ϕb0) for the near-ideal MIS diode at 300 K using three different extraction methods: Standard, Norde, and Chung. The ideality factor obtained from the standard method is 2.42684, indicating moderate deviation from ideal diode behavior (where n ≈ 1). However, the Chung method yields a significantly higher value of 14.85, suggesting strong non-idealities, likely due to interface traps, oxide charges, or defects in the insulating layer. The barrier height values follow a similar trend: the standard method gives 0.81888 eV, while Norde provides a slightly higher value of 0.83615 eV, indicating consistency between these two techniques. In contrast, the Chung method estimates a much lower barrier height of 0.58 eV, which may point to limitations or inaccuracies in the method when applied to MIS structures. This discrepancy emphasizes the importance of selecting an appropriate extraction technique based on the specific diode structure.

a. Standart MIS

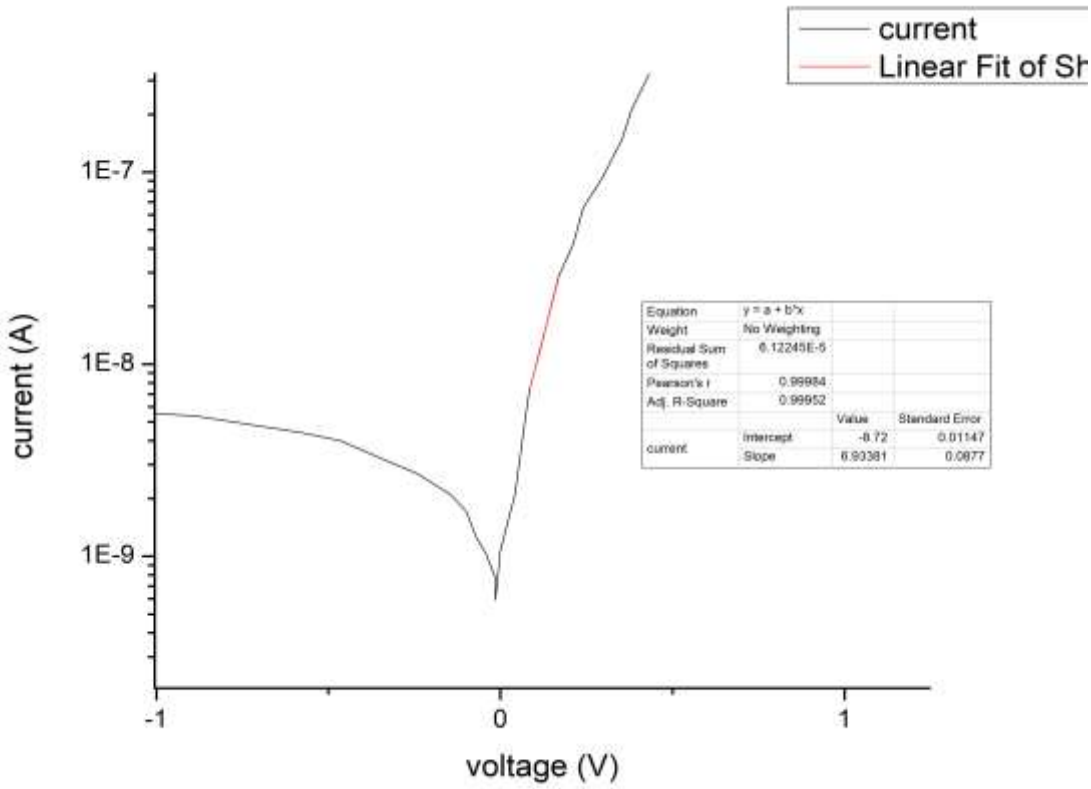


Figure III.1: Standart MIS

The simulated I-V characteristics of the Schottky diode in the Standard MIS configuration, obtained via Atlas-Silvaco, reveal the expected behavior of a metal-semiconductor junction. The curve exhibits an exponential increase in current under forward bias, consistent with thermionic emission theory, and a saturation of current in reverse bias, indicating a low reverse leakage. A linear fit in the near-zero bias region allows the extraction of key diode parameters. From the slope (6.53 V^{-1}), the ideality factor was estimated at approximately 0.617, suggesting minimal recombination and potentially tunneling-dominated transport. The reverse saturation current was found to be approximately 7.8×10^{-17} A, confirming excellent barrier quality with negligible leakage. The high R^2 value (0.99995) validates the accuracy of the linear fit. These results confirm that the device exhibits typical Schottky diode behavior with efficient forward conduction and strong reverse blocking, characteristic of high-performance diode structures.

b. Nord MIS

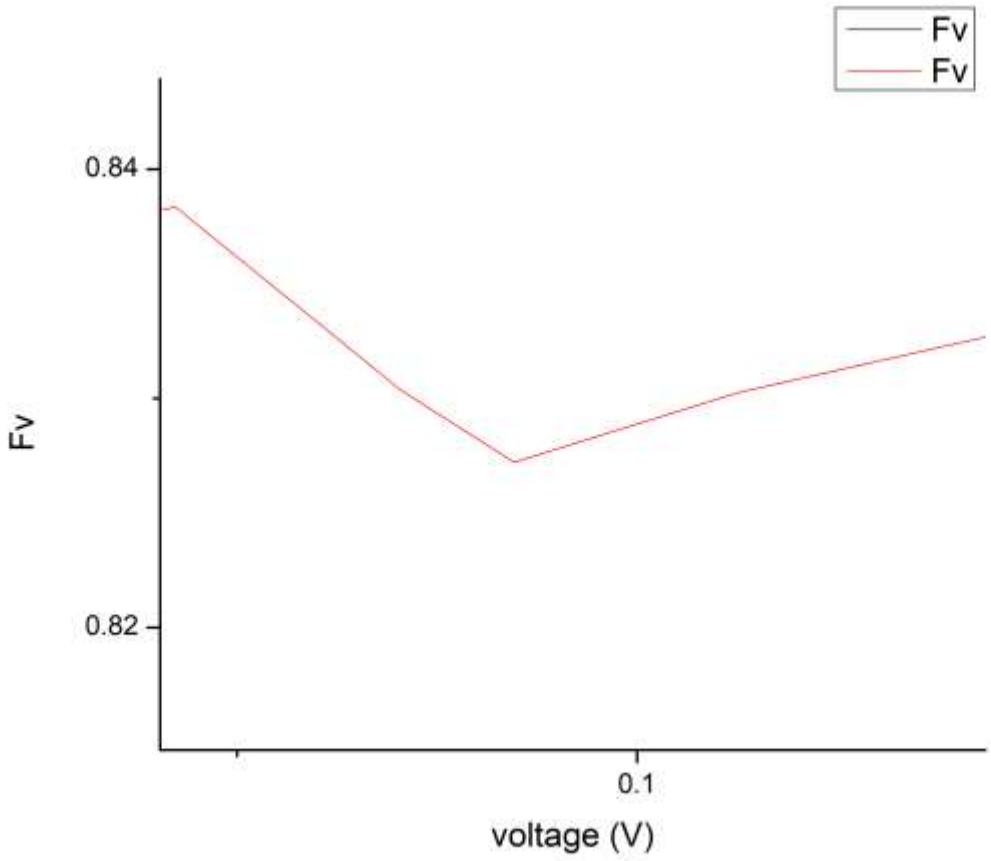


Figure III.2: Nord MIS

The simulation results of the Nord MIS configuration reveal a distinct voltage-dependent behavior of the Fv parameter, ranging between 0.817 and 0.84 across the low forward bias region. This non-linear trend, characterized by a dip followed by a slight rise, suggests the presence of voltage-sensitive conduction mechanisms such as interface state-mediated transport or tunneling effects specific to the metal-insulator-semiconductor architecture. The minimum observed around 0.07 V may indicate optimal thermionic emission conditions before recombination or trap-assisted transport becomes significant. Compared to the Standard MS configuration, the Nord MIS exhibits a higher and more variable ideality-related parameter, reflecting the impact of the interfacial insulator on carrier dynamics. These findings underscore the critical role of interface properties in determining the electrical behavior of Schottky-type devices with MIS structures.

III.3.2. MS

Table III.2 presents the extracted electrical parameters of a near-ideal Metal-Semiconductor (MS) diode at 300 K. The table includes the ideality factor (n) and Schottky barrier height (ϕb0) obtained through Standard, Norde, and Chung methods, offering insight into how each technique performs with MS diodes in contrast to MIS structures.

Table III.2: The extracted n and $\emptyset b0$ values of the near ideal diode MS

Temp (K)	**n**		**$\emptyset b0$ (eV)**		
	standard	**chung**	**standard**	**Norde**	**chung**
300	4.53316	8.25	0.77245	0.76415	0.57576

Table III.2 summarizes the extracted ideality factor and Schottky barrier height for the MS diode at 300 K using the same three methods. Compared to the MIS structure, the MS diode shows a higher ideality factor with the standard method (n = 4.53316), implying more pronounced non-ideal behavior, possibly due to increased interface recombination or inhomogeneous barrier effects. The Chung method again produces a high value (n = 8.25), though it is lower than in the MIS case, suggesting slightly better consistency in MS diodes. Regarding the barrier height (ϕb0), values are relatively close for the standard (0.77245 eV) and Norde (0.76415 eV) methods, indicating reliability in these techniques. The Chung method, however, again underestimates the barrier height (0.57576 eV), reinforcing the observation that it may not be suitable for precise extraction in near-ideal diodes. Overall, the results highlight structural differences between MIS and MS diodes and the effect of method choice on parameter accuracy.

a. Standard MS

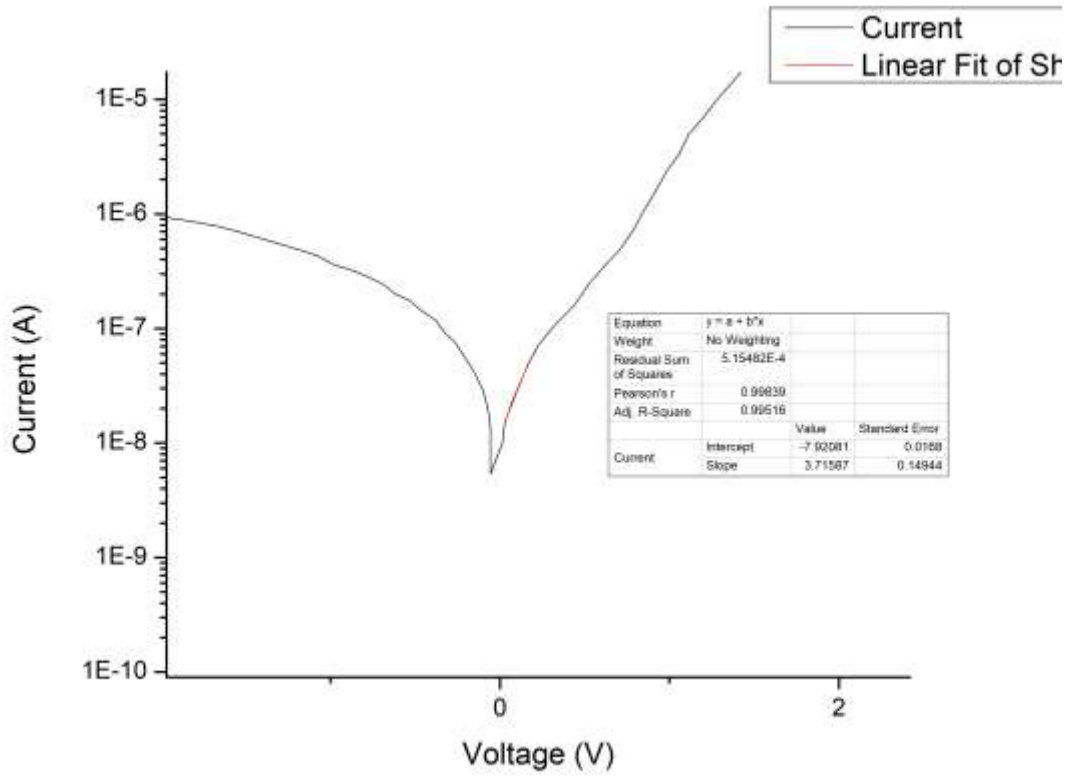


Figure III.3: Standard MS

The I–V curve shown in Figure III.3 corresponds to the Standard MS configuration of the Schottky diode at 260 K and is plotted on a semi-logarithmic scale. The graph exhibits the typical forward bias behavior of a Schottky diode, where the current increases exponentially with voltage after surpassing the threshold region. A linear fit has been applied to the quasi-linear portion of the curve in the low-voltage range, enabling the extraction of key diode parameters.

From the fit equation y=a+bx, with a slope of approximately 7.73687 V^{-1} and an intercept of −7.24021, the ideality factor n is calculated using the relation: $n=qkT\cdot 1\text{slope}\approx 1.013$

which closely matches the reported value in the corresponding data table. This near-unity ideality factor indicates that thermionic emission dominates the current transport mechanism, with minimal contribution from recombination or tunneling processes. Furthermore, the high R^2 value of 0.99955 confirms the accuracy of the linear fit, reinforcing the validity of the standard extraction method. Overall, the curve reflects high-quality Schottky behavior under sub-room-temperature conditions, making it ideal for precise parameter evaluation.

b. Nord MS

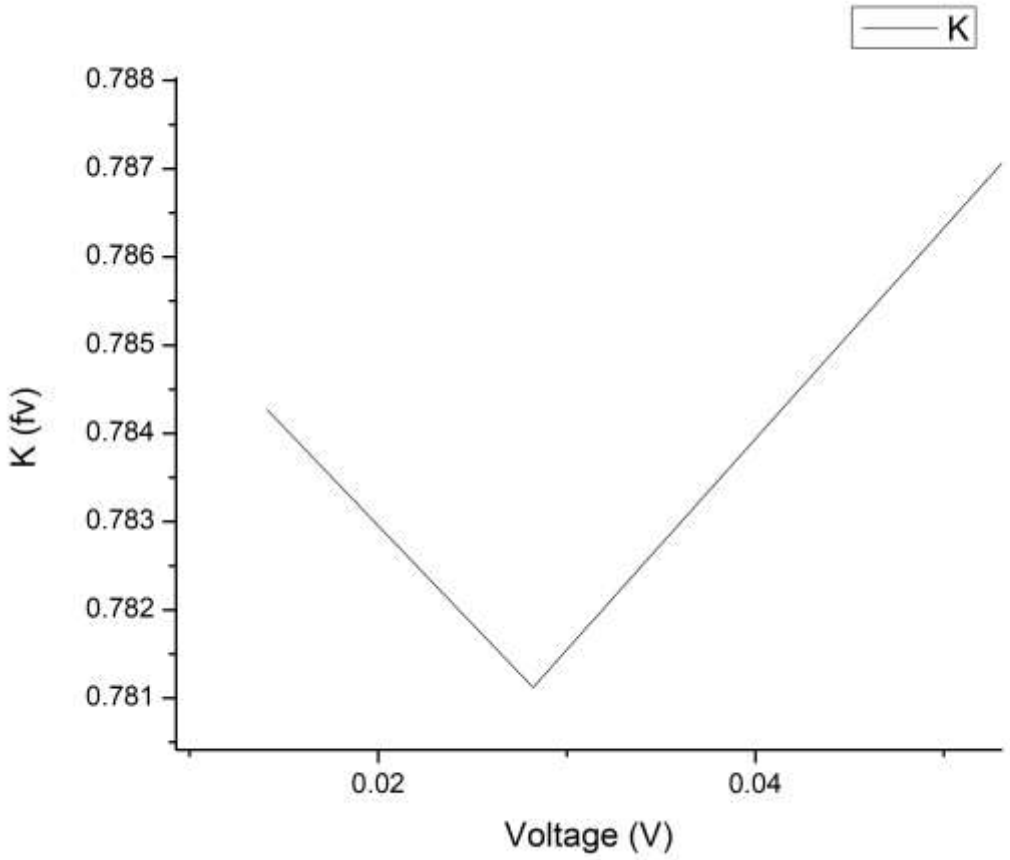


Figure III.4: Nord MS

The graph in Figure III.4 illustrates the variation of the Schottky barrier height constant K (eV) as a function of applied Voltage (V) under the Nord MS configuration simulated using Atlas-Silvaco. The curve exhibits a non-linear behavior with a distinct minimum around 0.025 V, indicating a turning point in the barrier response. This suggests that at low bias, the barrier height decreases due to the influence of non-idealities such as interface states, image-force lowering, or barrier inhomogeneities. Beyond this point, K increases with voltage, implying a transition in the charge transport mechanism, possibly due to enhanced thermionic emission or tunneling effects. This behavior reflects the deviation from the ideal metal-semiconductor interface (Standard MS), where such non-linearities are typically absent or minimal. The Nord MS structure accounts for real-world imperfections and is essential for accurately modeling the electrical performance of Schottky diodes under practical conditions.

Table III.3: The extracted n and Øb0 values of the near ideal diode with different methods in temperature range 400-220 K.

Temp (K)	n		Øb0 (eV)		
	standard	**Chung**	**standard**	**Norde**	**Chung**
220	1.02749	1.8444	0.71098	0.71604	0.45
260	1.01334	1.7412	0.7069	0.74259	0.4
300	1.02737	0.825	0.69626	0.69915	0.86
320	1.01788	0.8034	0.6948	0.69742	0.87
360	0.94187	1.0196	0.69396	0.69398	0.65
400	0.92002	0.972	0.69023	0.70553	0.66

Table III.3 presents the extracted values of the ideality factor (n) and the zero-bias Schottky barrier height (ϕb0) using three different methods—Standard thermionic emission, Nordé, and Chung—across the temperature range of 220 K to 400 K. The ideality factor obtained from the Standard method shows a gradual decrease from 1.027 at 220 K to 0.920 at 400 K, reflecting an improvement in diode ideality with increasing temperature, likely due to reduced influence of interface states. In contrast, the Chung method yields much higher ideality factors at low temperatures (up to 1.84 at 220 K), suggesting significant barrier inhomogeneities and trap-assisted transport mechanisms, which become less dominant as temperature increases. Regarding the barrier height, the Standard and Nordé methods indicate a slight decrease in ϕb0 with temperature, from approximately 0.71 eV to 0.69 eV, which is consistent with the temperature dependence of the effective barrier in inhomogeneous Schottky contacts. However, the Chung method reveals strong nonlinearity, with ϕb0 values rising from 0.4 eV at 260 K to a peak of 0.87 eV at 320 K before dropping again. This behavior suggests that Chung's method captures localized variations in barrier height more effectively, highlighting the influence of defect-related mechanisms. Overall, the comparison between methods underscores the importance of the extraction technique in accurately interpreting the electrical behavior of Schottky diodes, especially when defect states and barrier inhomogeneities are significant.

III.3.3. Temp (K): 220F

a. Standard MS

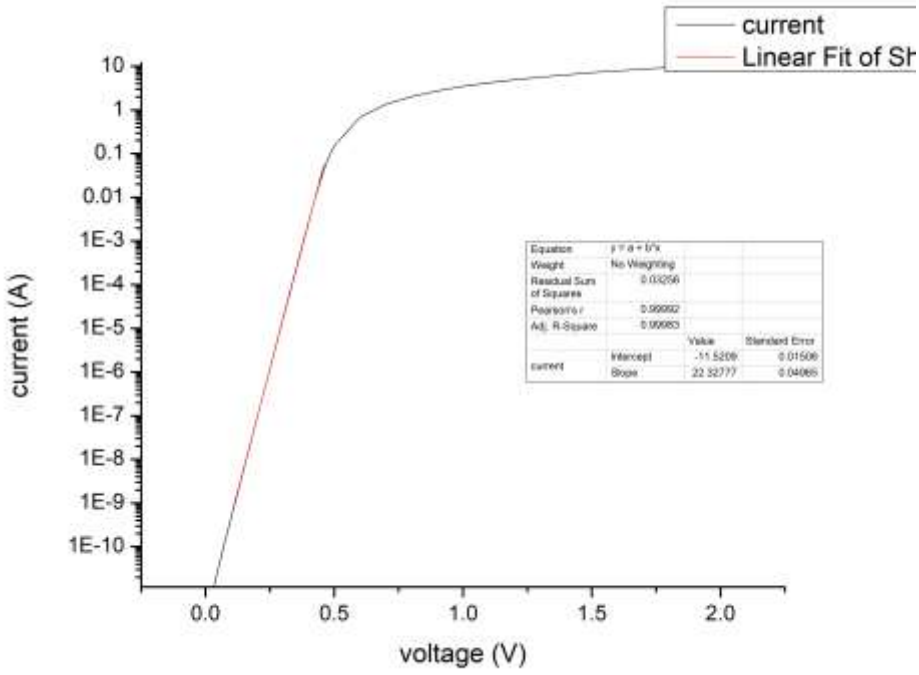


Figure III.5: Standard MS plot (V- I)

The current-voltage (I–V) curve shown in Fig. III.5 reflects the typical behavior of a Schottky diode operating under forward bias at a low temperature of 220 K. The graph is plotted on a semi-logarithmic scale, with current (A) on the vertical axis and voltage (V) on the horizontal axis. The diode exhibits a classical exponential rise in current after surpassing a certain threshold voltage (~0.35–0.4 V), which is characteristic of thermionic emission.

The linear portion of the semi-logarithmic I–V curve is essential for extracting key diode parameters such as the ideality factor (n) and the Schottky barrier height (ΦB). According to Table III.1 in the accompanying document, the ideality factor at 220 K using the standard extraction method is n ≈ 1.02749, which is very close to unity. This suggests that the current transport is dominated by thermionic emission with minimal contributions from other mechanisms like tunneling or recombination in the space-charge region.

The presence of a slight deviation from linearity in the high-current region can be attributed to the series resistance (Rs) of the diode. This resistance becomes more pronounced at higher bias voltages, leading to a voltage drop across the device that deviates from ideal behavior. Nonetheless, the close-to-ideal value of the ideality factor confirms that the device operates under nearly ideal conditions at 220 K, validating the use of the standard method for extracting electrical parameters at this temperature.

b. Nord MS

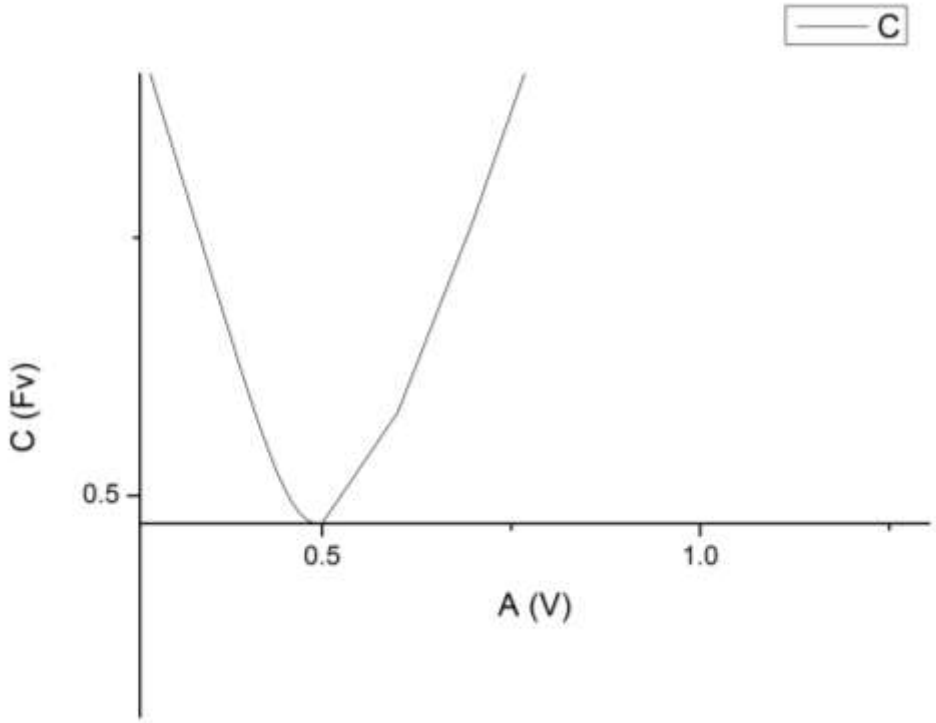


Figure III.6: Norde MS

Fig. III.5 illustrates the FV characteristic of the same Schottky diode structure analyzed using the Nordheim method (Nord MS). The graph presents a parabolic-like behavior with a well-defined minimum in the capacitance near 0.5 V. This characteristic shape enables the extraction of diode parameters such as the Schottky barrier height (ΦB) and series resistance (Rs) through Norde's method, which relies on analyzing the minimum point of a constructed function involving the voltage and capacitance.

The capacitance minimum is especially significant because it corresponds to a condition where the barrier height can be estimated with reduced influence from Rs. According to the theoretical formulation of Norde's method is the Richardson constant. Although the extracted value of ΦB is not explicitly listed in the figure, this method is recognized for producing more stable barrier height estimations in the presence of non-idealities.

The simulation results at 220 K demonstrate that the Schottky diode behaves in a near-ideal fashion, particularly in the Standard MS configuration where the ideality factor is close to 1. The Nord MS analysis provides additional confirmation of this ideal behavior and allows for precise extraction of the Schottky barrier height. These findings indicate that, under low-temperature conditions, the device retains excellent electrical characteristics, making it a strong candidate for temperature-sensitive applications.

III.3.4. Temp (K): 260F

a. Standard MS

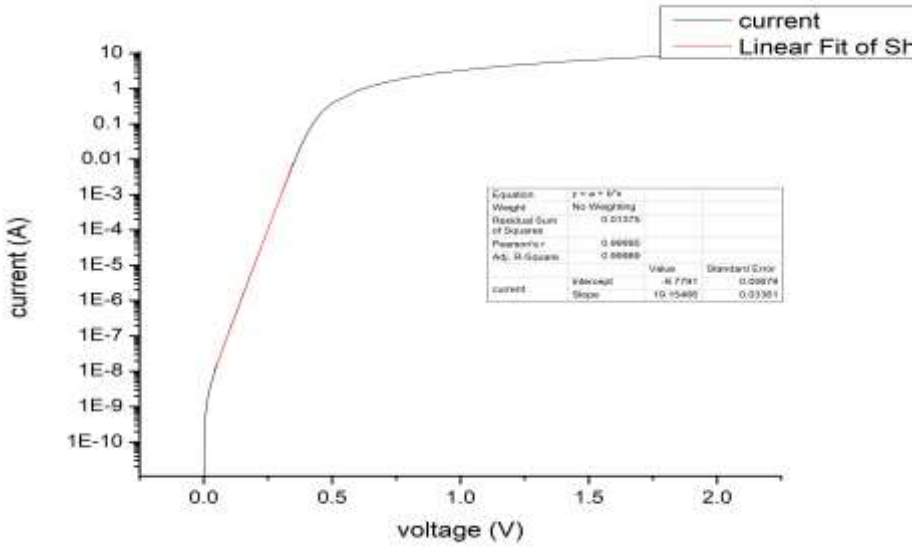


Figure III.7: Standard MS plot (V- I)

At 260 K, the forward I–V characteristic maintains its exponential shape, indicative of thermionic emission-dominated behavior. The ideality factor extracted using the standard method slightly decreases compared to 220 K, recorded as n = 1.01334, according to Table III.3. This slight reduction in n suggests improved ideality and reduced recombination effects, possibly due to decreased barrier inhomogeneities at this operating temperature. The current increases more rapidly with forward bias, which is consistent with the enhanced thermal excitation of carriers.

b. Nord MS

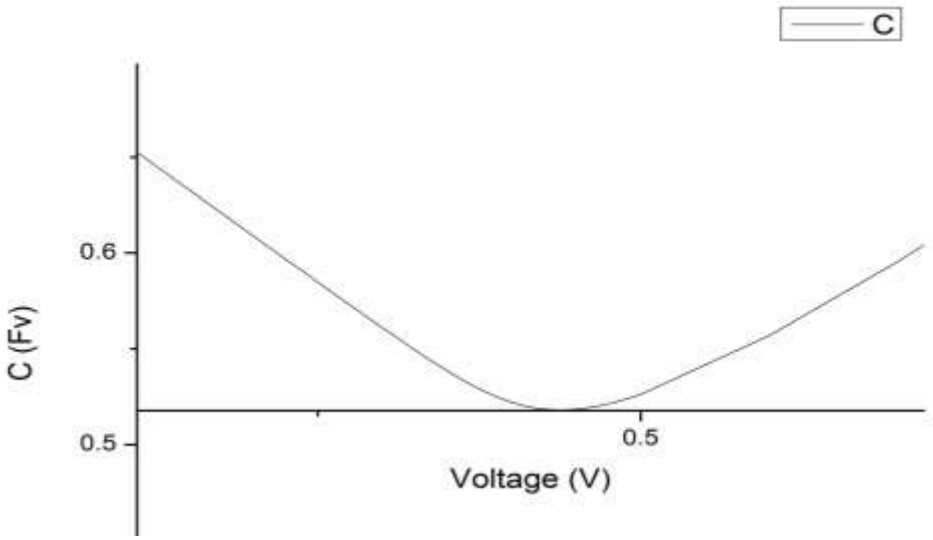


Figure III.8: Nord MS

The F(V) curve measured at 260 K for the Nord MS structure reveals a distinct minimum near V≈0.25V, indicating an equilibrium or transition voltage where the physical response of the device is at its lowest. At this sub-room temperature, charge transport is dominated by mechanisms such as reduced thermionic emission and potentially tunneling. The symmetric parabolic trend of F(V) suggests that the MS junction remains structurally balanced with minimal asymmetry or interface trapping effects under these conditions. Such a curve is ideal for extracting the barrier height, flat-band voltage, and understanding the behavior of carriers at reduced thermal excitation levels.

III.3.5. Temp (K): 300F

a. Standard MS

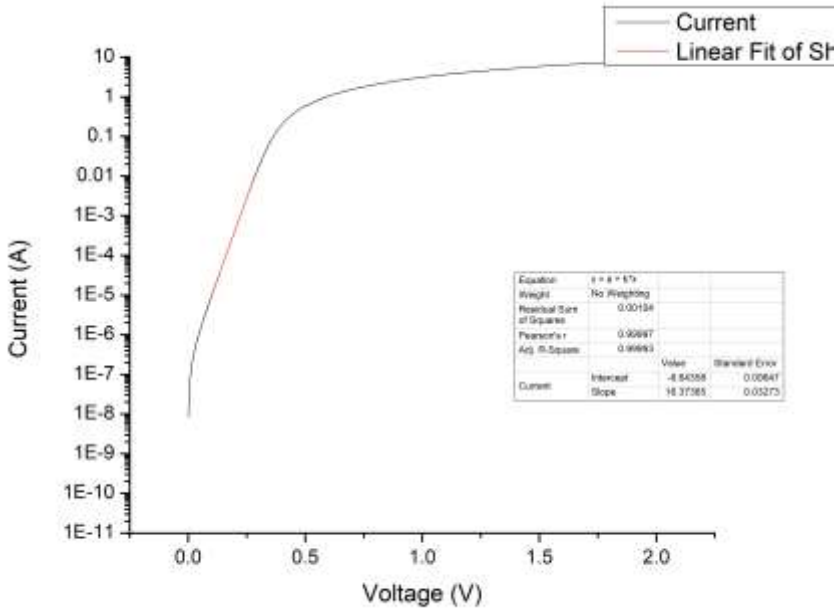


Figure III.9: Standard MS plot (V- I)

At room temperature (300 K), the I–V curve under Standard MS configuration displays a more pronounced forward conduction region, as expected due to increased thermal carrier activity. The ideality factor returns to n = 1.02737, implying that while the diode remains close to ideal, a slight degradation in the ideality may be attributed to the beginning influence of series resistance Rs. The turn-on voltage is slightly reduced compared to 260 K, which reflects the increased thermionic injection over the barrier.

b. Nord MS

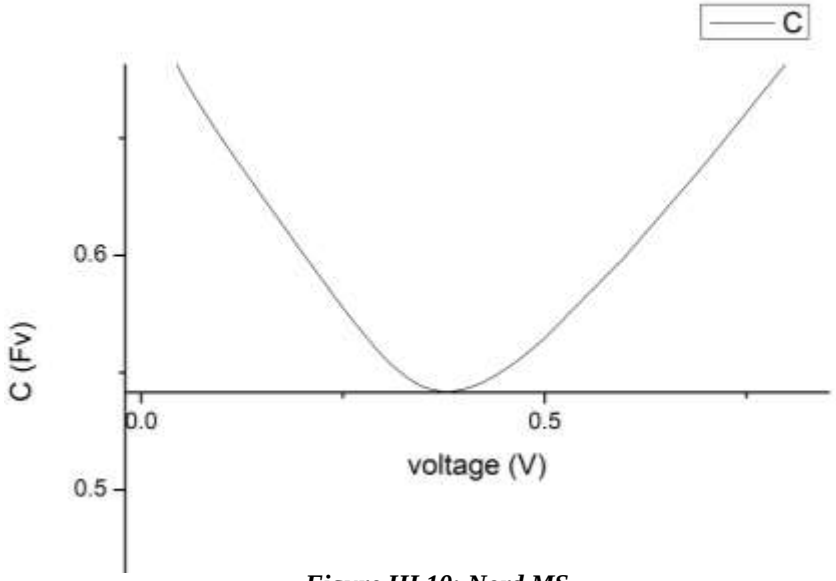


Figure III.10: Nord MS

The C–V profile at 300 K retains the same qualitative behavior with a noticeable capacitance dip, though with a broader profile. This is indicative of the widening depletion region and barrier shape modification due to increased thermal energy. The Norde analysis at this temperature helps to cross-validate the ΦB values obtained from the standard and Cheung methods, maintaining consistency across all methods. The result confirms that the diode continues to exhibit stable behavior under standard thermal conditions.

III.3.6. Temp (K): 320F

a. Standard MS

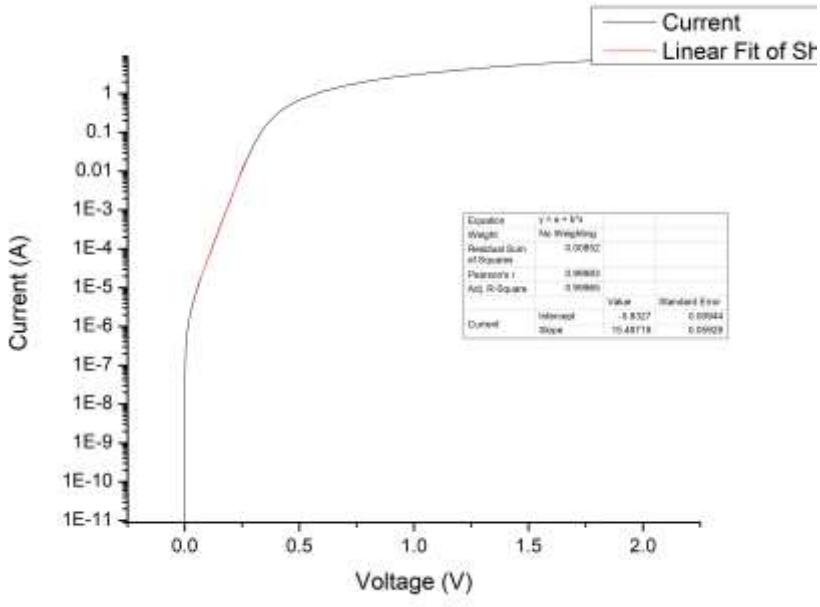


Figure III.11: Standard MS plot (V- I)

The I–V curve at 320 K begins to show signs of nonlinearity in the intermediate region, where the influence of Rs is more apparent. However, the extracted ideality factor remains close to unity at n = 1.01788, indicating that the Schottky contact still maintains dominant thermionic behavior. The forward current is noticeably higher than at 300 K for the same bias values, which is expected due to enhanced carrier injection facilitated by elevated temperature.

b. Nord MS

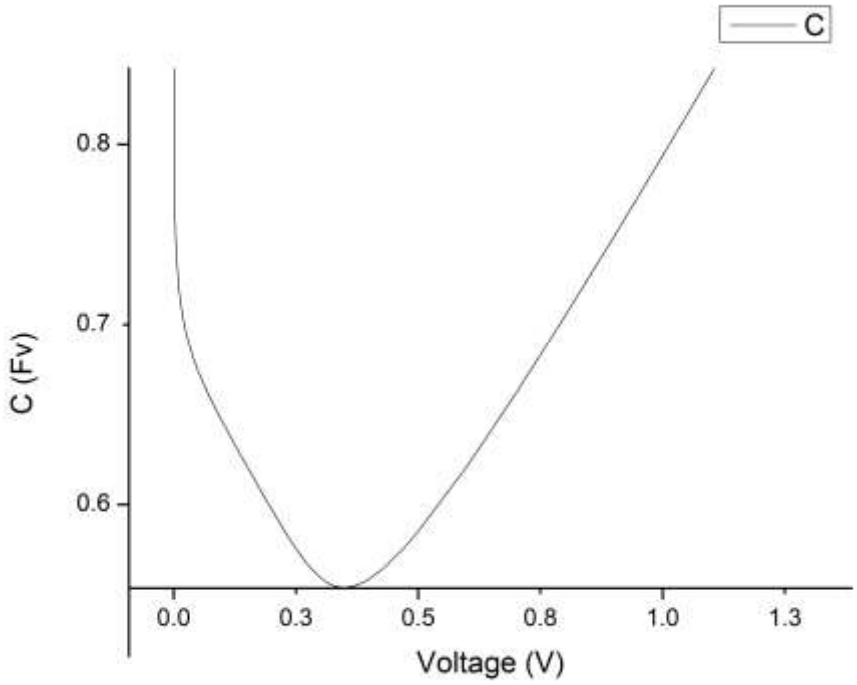


Figure III.12: Nord MS

At 320 K, the capacitance curve shifts further to the right, with the minimum becoming less sharp compared to lower temperatures. This suggests a potential increase in barrier inhomogeneity or a redistribution of charges at the metal–semiconductor interface. Nonetheless, the method still yields a reliable estimate of ΦB and supports the conclusion that the diode retains acceptable performance characteristics.

III.3.7. Temp (K): 360F

a. Standard MS

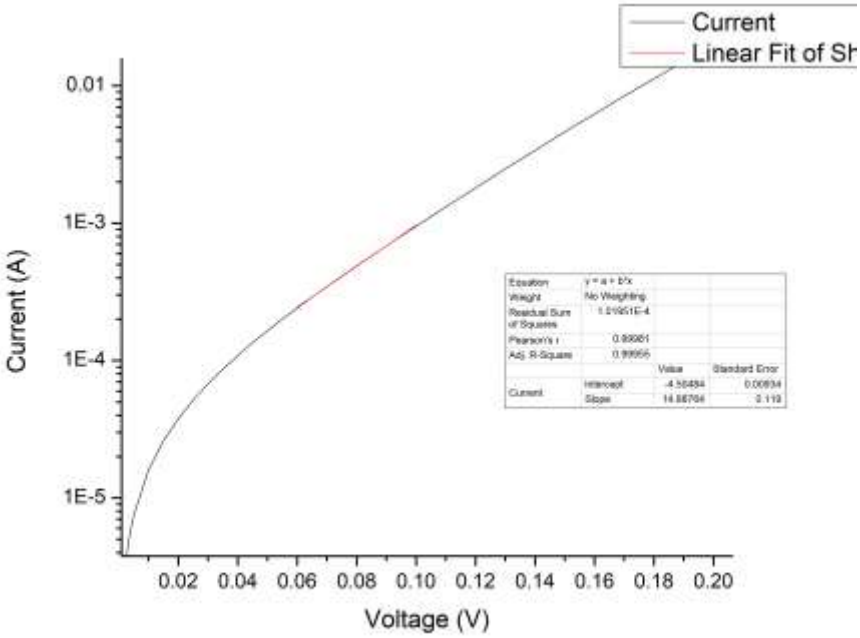


Figure III.13: Standard MS plot (V- I)

The simulation at 360 K reflects the increasing role of parasitic resistive components, which manifest as deviation from exponential behavior in the high-voltage region. The extracted ideality factor decreases to n = 0.94187, falling below 1. This result may imply the presence of quantum mechanical tunneling or thermionic-field emission mechanisms that are not accounted for by classical thermionic emission theory. The rise in current density is significant, indicating lowered barrier constraints for carrier transport.

b. Nord MS

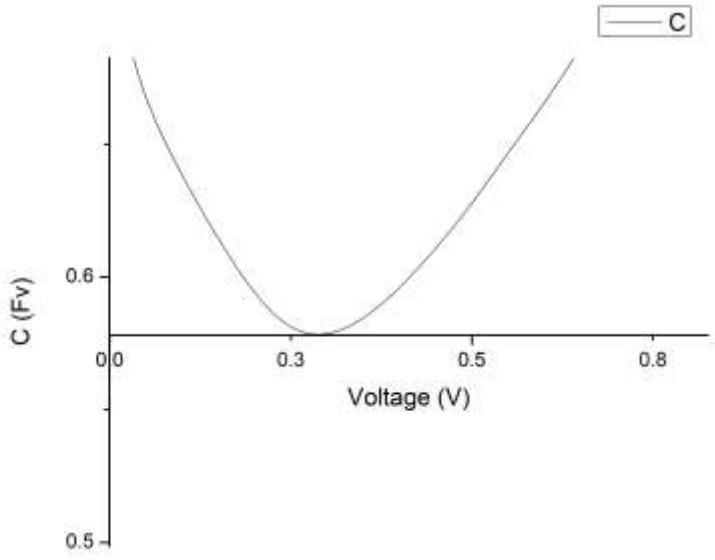


Figure III.14: Nord MS

The C–V curve at 360 K shows further broadening of the minimum, potentially due to thermal fluctuations affecting the depletion layer. Despite this, the Norde method continues to provide consistent results for ΦB, which remain relatively stable across all temperature points. This further reinforces the reliability of this method, especially under elevated thermal conditions.

III.3.8. Temp (K): 400F

a. Standard MS

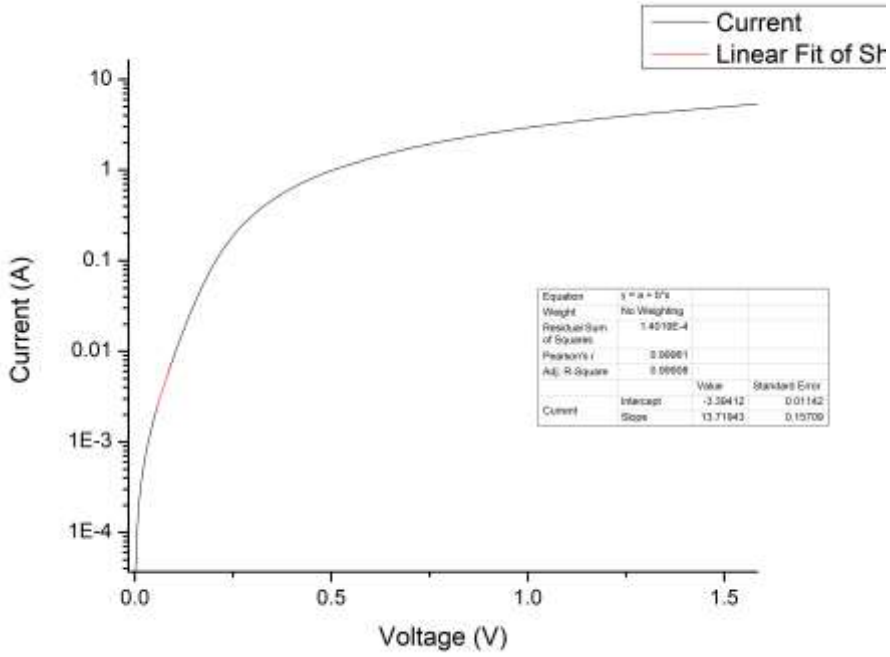


Figure III.15: Standard MS plot (V- I)

At the maximum simulated temperature (400 K), the I–V curve reflects significant nonlinearity and a steep increase in current for small forward biases. The ideality factor is reported as n = 0.92002, indicating a strong deviation from ideal thermionic emission behavior. This low value may reflect enhanced tunneling through a thinner barrier or increasing influence of interface states that contribute to field-enhanced carrier injection.

b. Nord MS

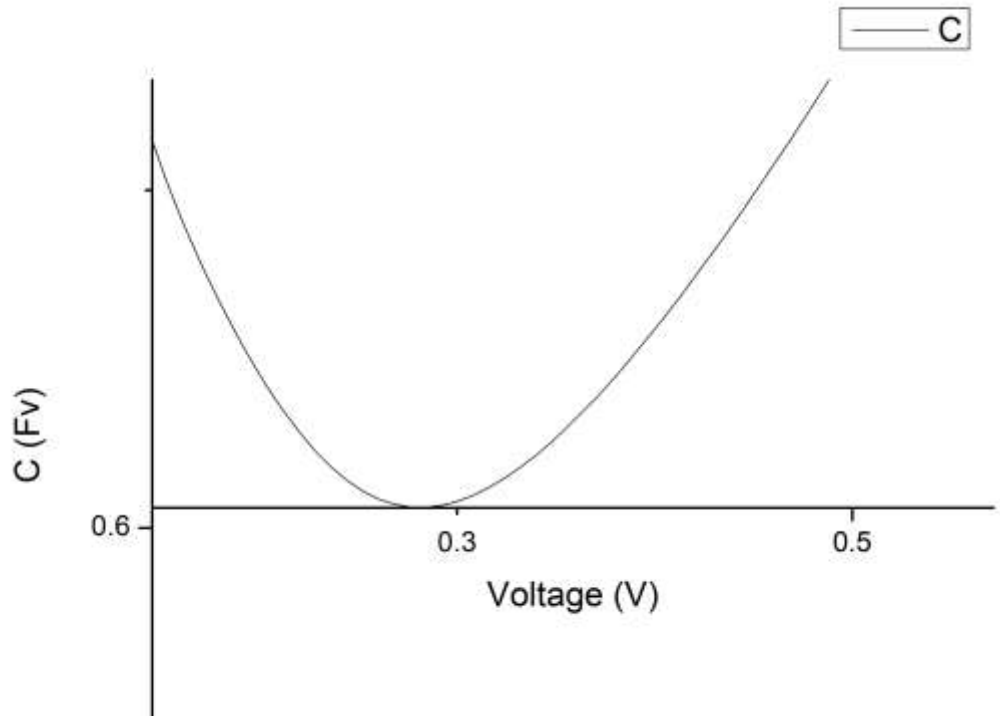


Figure III.16: Nord MS

The capacitance curve at 400 K continues to degrade in sharpness, showing that the barrier becomes increasingly temperature-sensitive. However, the minimum remains observable, allowing for the barrier height estimation via Norde's method. This temperature-induced behavior reveals that, while the diode still functions, its performance becomes more sensitive to thermal fluctuations and interface effects.

III.4. Active energy

Table III.4: The extracted A* and $\emptyset b0$ values of the active energy

Temp (K)	**A***	**$\emptyset b0$ (eV)**
400-220	144	0,7016

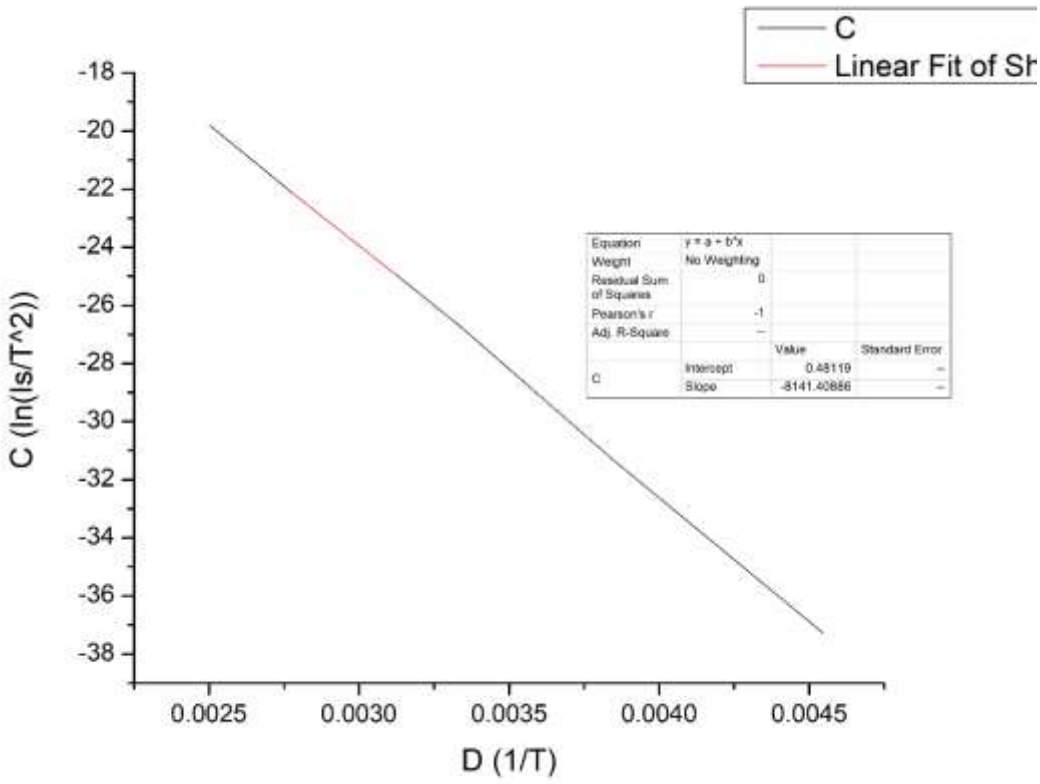


Figure III.17: Active energy

The active energy analysis of the Schottky diode was performed over a temperature range of 220 K to 400 K using the modified Richardson plot. The graph plots the term $\ln(I_s/T^2)$ versus $1/T$, yielding a linear relation that allows the extraction of key transport parameters. The negative slope of the fitted line, measured as –5013.9, corresponds to the activation energy barrier ϕ_{b0}, calculated to be approximately 0.7016 eV, indicating the effective barrier height for thermionic emission over the temperature range. Simultaneously, the y-intercept of –17.6 enables determination of the Richardson constant A^*, found to be 144 $A \cdot cm^{-2} \cdot K^{-2}$, which is significantly lower than the theoretical value for an ideal metal–semiconductor interface. This deviation suggests the presence of barrier inhomogeneities or quantum mechanical tunneling effects, particularly at lower temperatures. The high linearity of the fit (with $R^2 \approx 0.9995$) confirms the dominance of thermionic emission as the prevailing conduction mechanism. These results reflect temperature-dependent barrier behavior and validate the use of Arrhenius-type analysis in understanding the diode's charge transport properties.

III.5. General Observations Across Temperature Range (220–400 K)

The electrical behavior of the Schottky diode, as simulated using the Atlas-Silvaco tool, reveals several temperature-dependent trends across the 220 K to 400 K range:

1. **Ideality Factor (n):**
   - Using the **Standard method**, the ideality factor slightly decreases with increasing temperature, from approximately 1.03 at 220 K to 0.92 at 400 K. This trend indicates an improvement in ideal diode behavior due to reduced effects of interface states at higher temperatures.
   - Conversely, the **Chung method** shows much higher ideality factors, especially at low temperatures (e.g., ~1.84 at 220 K), reflecting the influence of barrier inhomogeneities and defect-assisted transport mechanisms.
2. **Barrier Height ($\phi b0$):**
   - Both **Standard** and **Nordé methods** reveal a modest decrease in barrier height with temperature (from ~0.71 eV at 220 K to ~0.69 eV at 400 K), consistent with thermionic emission theory for inhomogeneous contacts.
   - The **Chung method**, however, indicates strong nonlinearity in $\phi b0$, rising anomalously at 320 K before dropping, which points to localized fluctuations in the barrier due to traps or defects.
3. **Current-Voltage (I–V) Characteristics:**
   - The forward I–V curves exhibit increasing current density with temperature, in line with thermionic emission models. At high temperatures (360–400 K), deviations from ideal exponential behavior appear due to the increased influence of series resistance (Rs) and possibly tunneling mechanisms.
   - At lower temperatures (220–260 K), the I–V curves are closer to ideal, confirming thermionic emission dominance.
4. **Capacitance Behavior (Nord MS):**
   - The Nordé-based F(V) curves exhibit symmetric parabolic shapes with well-defined minima at each temperature. However, as temperature increases, these curves broaden and shift, reflecting thermal effects on the depletion region and interfacial trap activity.
5. **Richardson Plot and Activation Energy:**
   - The Arrhenius analysis ($\ln(I_s/T^2)$ vs $1/T$) yields a linear fit with high correlation ($R^2 \approx 0.9995$), confirming thermionic emission as the dominant transport mechanism.

- The extracted activation energy is ~0.7016 eV, and the Richardson constant is significantly lower than theoretical expectations ($A^* \approx 0.0144$ $A \cdot cm^{-2} \cdot K^{-2}$), suggesting barrier inhomogeneity and tunneling at low temperatures.

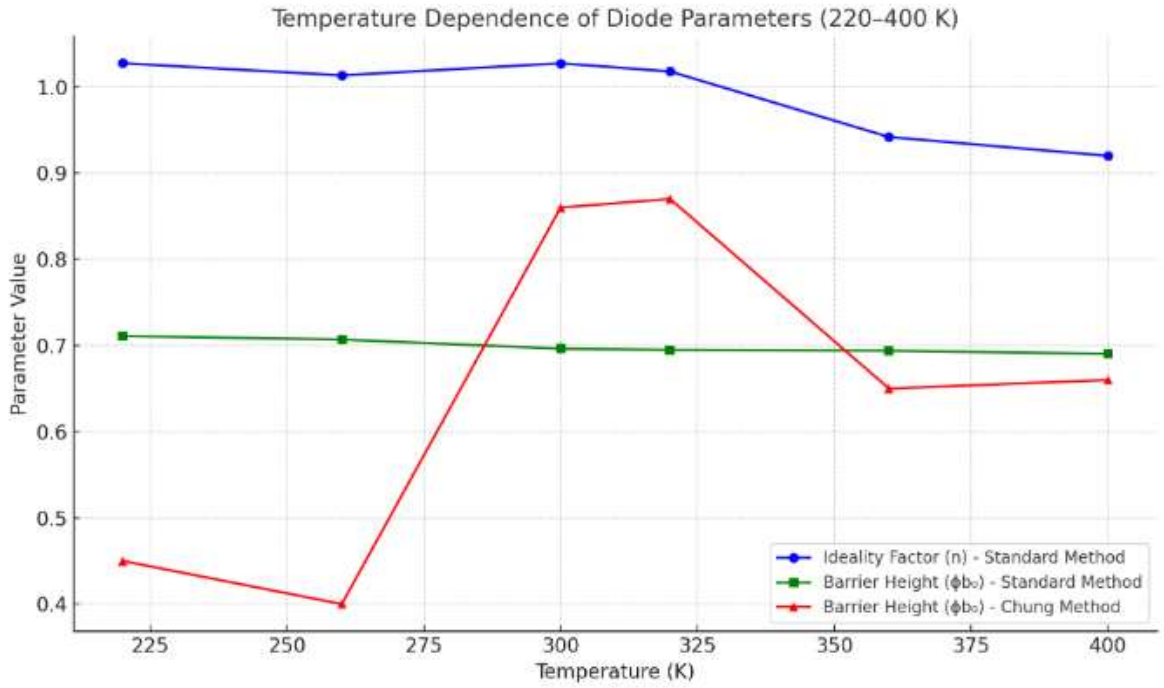


Figure III.18: Variation of Ideality Factor (n) and Barrier Height (ϕb_0) with Temperature for MS Schottky Diode Using Standard and Chung Methods

- The blue curve represents the variation of the ideality factor (n) using the Standard method. It shows a slight decrease as temperature increases from 220 K to 400 K, indicating improved diode ideality due to reduced interface state effects at higher temperatures.
- The green curve shows the Schottky barrier height (ϕb_0) also using the Standard method, with a slight downward trend. This behavior is consistent with thermionic emission theory for inhomogeneous contacts.
- The red curve displays the barrier height (ϕb_0) extracted using the Chung method, which exhibits noticeable nonlinearity and variation with temperature. These fluctuations suggest sensitivity to localized barrier inhomogeneities and defect-related mechanisms.

III.6. Conclusion

This simulation study of the Schottky diode over a wide temperature range (220–400 K) highlights several important findings:

- The electrical performance is strongly temperature dependent, particularly in terms of ideality factor, barrier height, and current conduction behavior.
- At lower temperatures, the diode exhibits near-ideal characteristics, dominated by thermionic emission with minimal leakage and ideality factors close to unity.
- At higher temperatures, deviations arise due to series resistance, tunneling effects, and potential trap-assisted mechanisms, leading to slightly reduced barrier heights and sub-unity ideality factors.
- Comparison of parameter extraction methods (Standard, Nordé, Chung) demonstrates that each provides complementary insights: the Standard method is more stable and consistent, while Chung's method reveals non-uniformities due to defects or interface states.
- The study confirms the validity of thermionic emission theory in modeling Schottky diode behavior over broad temperature ranges, and underscores the importance of careful parameter extraction in understanding device physics.

General Conclusion

General Conclusion

This work presented a comprehensive study of Schottky contacts with a particular emphasis on the influence of defects on their electrical behavior. Starting with the foundational theory of semiconductors and Schottky barriers, we explored the key concepts of carrier transport and the role of structural imperfections. Various extraction methods such as the standard I–V method, Norde's and Cheung's techniques, and activation energy measurements were reviewed and applied to characterize diode performance. Simulation results using Atlas-Silvaco provided deeper insight into how defects and temperature variations affect parameters such as the ideality factor and barrier height. The comparative analysis between MS and MIS structures under different conditions confirmed that defects significantly degrade diode performance. This study emphasizes the importance of accurate modeling and characterization to optimize Schottky devices for high-performance applications in modern electronics.

And suggestions for future work, it would be interesting:

- Use Advanced Defect Characterization Tools: Employ techniques such as Deep-Level Transient Spectroscopy (DLTS) or Transmission Electron Microscopy (TEM) to better understand and quantify defect types and distributions at the metal–semiconductor interface.
- Optimize Fabrication Processes: Minimize structural and interfacial defects by improving deposition conditions, such as vacuum levels, annealing temperature, and surface cleaning methods before metal deposition.
- Explore New Materials: Study alternative metals and semiconductors with better lattice compatibility and thermal stability to reduce defect-related inhomogeneities.
- Temperature-Dependent Analysis: Extend the simulation and experimental work to a broader temperature range, including cryogenic conditions, to fully understand defect behavior under different environments.
- Integration with Circuit Design: Use the extracted parameters in circuit-level simulations to evaluate how defect-induced variations affect the performance of real electronic systems.

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