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Presented by:

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Contribution to the Study of the Performance of Z-Source Converters

Thesis publicly defended on **19th December 2024**

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Dedication

I dedicate this work to

To my parents, Khalifa and Massouda, for their unwavering love, endless support, and belief in my abilities.

To my wife, Noussaiba, for your unwavering love, understanding, and countless sacrifices. You are my rock.

To my dearest children, Siloune, Bissane and Ahmed rayane. This is for you.

To my sisters and brothers, and to all my family

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List of Publications

Publications in refereed conferences

- **A.Abid**, L.Zellouma, R.Boualga "High Efficiency Impedance Z-source Inverter Operating in Stand-alone Mode" AAS Summer university **2019**,Universite BATNA-2
- **A. Abid**, L. Zellouma, M. Bouzidi, A. Lashab and B. Rabhi, "Switched Inductor Z-source/quasi Z-source Network: State of Art and Challenges," 020 1st International Conference on Communications, Control Systems and Signal Processing (CCSSP), EL OUED, Algeria, **2020**, pp. 477-482
- **A. Abid**, L. Zellouma, M. Bouzidi, A. Lashab, M.T. Boussabeur and B. Rabhi A Comparative Study of Recent Discontinuous Modulation Techniques for Three-Phase Impedance Source Inverter" the 13th Seminar on Power Electronics and Control (SEPOC **2021**), Brazil

Publications in refereed journals

- **A. Abid**, A. Bakeer, L. Zellouma, M. Bouzidi, A. Lashab, and B. Rabhi, "Low Computational Burden Predictive Direct Power Control of Quasi Z-Source Inverter for Grid-Tied PV Applications," **Sustainability**, vol. 15, no. 5, p. 4153, 2023.
- **Abid, A**.; Bakeer, A.; Albalawi, H.; Zellouma, L.; Bouzidi, M.; Lashab, A.; Rabhi, B.; Chub, A. Optimized Modulation Scheme for Four-Leg Quasi Z-Source Inverter: Reducing Power Loss and Improving Output Quality. **IEEE Access** 2023.

Abstract

The fact growing for advanced control strategies in Distributed Generation (DG) systems by harnessing the potential of Z-source inverters (ZSIs) and quasi-Z-source inverters (qZSIs) as a powerful type of Impedance Source Inverter (ISI). To achieve this, the research explores four key objectives. Firstly, a comparative analysis through simulations evaluates the ability of ZSI/qZSI with switched-inductors to boost voltage, considering factors like voltage gain and component count. Secondly, a comprehensive review assesses existing modulation techniques for ZSI/qZSIs. Thirdly, a novel three-dimensional space vector modulation (3DZSVM) technique specifically designed for four-leg qZSIs (4L-qZSIs) is introduced. This method improves overall performance, particularly in steady-state operation and reduced harmonic distortion. Finally, a novel simplified predictive direct power control (PDPC) strategy for grid-tied photovoltaic (PV) systems using qZSIs is proposed. This method operates with a fixed switching frequency and achieves superior power tracking and grid integration. The research presented here, substantiated by detailed explanations, analyses, and simulation results, advances the development of ZSI/qZSI control for DG systems, paving the way for their wider adoption in building robust and efficient renewable energy integration solutions.

Keywords: Distributed Generation (DG), Z-source inverter (ZSI), quasi-Z-source inverter (qZSI), Impedance Source Inverter (ISI), space vector modulation (SVM), Three dimensional space vector modulation (3DZSVM), predictive direct power control (PDPC), photovoltaic (PV), renewable energy integration, Computational burden, Power losses.

Abstract (in French)

Face à la demande croissante de stratégies de contrôle avancées dans les systèmes de génération distribuée (GD), cette thèse exploite le potentiel des onduleurs à source Z (ZSI) et des onduleurs quasi Z-source (qZSI) en tant que type puissant d'onduleur à source d'impédance (ISI). Pour atteindre cet objectif, la recherche explore quatre objectifs clés**.** Premièrement, une analyse comparative par simulations évalue la capacité des ZSI/qZSI avec des inductances commutées à élever la tension, en tenant compte de facteurs tels que le gain de tension et le nombre de composants. Deuxièmement, une revue complète évalue les techniques de modulation existantes pour les ZSI/qZSI. Troisièmement, une nouvelle technique de modulation vectorielle tridimensionnelle (3DZSVM) spécialement conçue pour les qZSI à quatre branches (4L-qZSI) est introduite. Cette méthode améliore les performances globales, en particulier en fonctionnement en régime permanent et en réduisant la distorsion harmonique. Enfin, une nouvelle stratégie simplifiée de contrôle direct de la puissance prédictive (PDPC) pour les systèmes photovoltaïques (PV) connectés au réseau utilisant des qZSI est proposée. Cette méthode fonctionne avec une fréquence de commutation fixe et permet un meilleur suivi de la puissance et une meilleure intégration au réseau. La recherche présentée ici, étayée par des explications détaillées, des analyses et des résultats de simulation, fait progresser le développement du contrôle ZSI/qZSI pour les systèmes DG, ouvrant la voie à leur adoption plus large dans la construction de solutions d'intégration d'énergie renouvelable robustes et efficaces.

Mots-clés : Génération distribuée (GD), Onduleur à source Z (ZSI), Onduleur quasi Z-source (qZSI), Onduleur à source d'impédance (ISI), Modulation vectorielle spatiale (SVM), Modulation vectorielle spatiale tridimensionnelle (3DZSVM), Contrôle direct de la puissance prédictive (PDPC), Photovoltaïque (PV), Intégration des énergies renouvelables, Charge de calcul, Pertes de puissance

Abstract (in Arabic)

الملخص

تزداد أنظمة التوليد الموزع (DG) اعتمادًا على استراتيجيات التحكم المتقدمة لدمج مصادر الطاقة المتجددة بشكل فعال . تعالج هذه الأطروحة هذه الحاجة من خلال استكشاف إمكانات مقومات المصدر Z (ZSIs) ومقومات المصدر Z شبه (qZSIs)كمقومات مصدر الإعاقة (ISIs) لتطبيقات التوليد الموزع.

يبحث البحث أربعة أهداف رئيسية:

1. **تحليل مقارن لطوبوغرافيات :ZSI/qZSI** يقيم تحليل يستند على المحاكاة قدرة ZSI/qZSI مع المحاثات المؤتلة على رفع الجهد .يحلل معايير رئيسية مثل مكسب الجهد وإجهاد مفتاح العاكس وعدد المكونات وتموج التيار الحثي.
2. **مراجعة استراتيجيات التعديل :**يتم إجراء مراجعة شاملة لاستراتيجيات التعديل الحالية لمقومات المصدر Z ثلاثية الطور .(ZSI/qZSIs) توفر هذه المراجعة تقييمًا مقارنًا لمزاياها وقيودها وملاءمتها للتطبيقات المختلفة.
3. **تعديل متجه الفضاء ثلاثي الأبعاد جديد :(3DZSVM)** يتم تقديم تقنية تعديل متجه الفضاء ثلاثي الأبعاد (SVM)جديدة مصممة خصيصًا لمقومات المصدر Z شبه رباعية الأرجل .(4L-qZSIs) تعمل هذه الطريقة، المسماة DZSVM3، على تحسين الأداء العام، خاصة في التشغيل في الحالة المستقرة وتقليل التشويه التوافقي .توضح المحاكاة مزايا كبيرة لـ DZSVM 3على تقنيات PWM القائمة على الناقل التقليدية.
4. **التحكم البسيط المباشر بالطاقة التنبؤية :(PDPC)** يتم اقتراح استراتيجية PDPC جديدة لأنظمة الفولطاضيائية المتصلة بالشبكة (PV) باستخدام qZSIs تعمل هذه الطريقة بتردد تبديل ثابت ولا حاجة إلى عامل ترجيح .إنها تستخدم تقنية تعديل متجهة فراغية مبسطة لاختيار ناقلات التبديل المثلى .تؤكد المحاكاة أن PDPC يتعقب ويولد الطاقة القصوى بفعالية من نظام PV ، حتى مع ديناميكيات متغيرة بسرعة .بالإضافة إلى ذلك ، فهي تضمن خرج الجهد المتردد المطلوب وتحكمًا فائقًا في كل من مراجعات القوة الفعالة والقوة التفاعلية مع تقليل تموج الطاقة.

الكلمات المفتاحية: التوليد الموزع(DG) , عاكس مصدر(ZSI) , عاكس شبه مصدر (qZSI) ,عاكس مصدر الإعاقة (ISI), تعديل متجه الفضاء (SVM), تعديل متجه الفضاء ثلاثي الأبعاد(3DZSVM), التحكم المباشر بالطاقة التنبؤية (PDPC) , الطاقة الشمسية الكهروضوئية(PV) , تكامل الطاقة المتجددة ,الحمل الحسابي, فقدان الطاقة.

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Nomenclature

Acronym	
RES	Renewable energy sources
PV	Photovoltaics source
PEC	Power Electronics Converters
VSI	Voltage source inverters
DC	Direct current
AC	Alternating current
ISI	Impedance source inverter
ZSN	Z-source network
ST	Shoot-through
ZSI	Z-source inverter
qZSI	Quasi Z-source inverter
MPPT	Maximum power point tracking
DG	Distributed generation
SL-ZSI	Switched Inductor Z-source inverter
SL-qZSI	Switched Inductor quasi Z-source inverter
VL-SL-qZSI	Switched Inductor quasi Z-source Inverter
SCL-qZSI	Switched coupled inductor quasi Z-source inverter
rSL-qZSI	Ripple Switched Inductor quasi Z-source inverter
cSL-qZSI	Continuous input current switched inductor quasi-Z-source inverter
SL-ISL-qZSI	Switched Inductor and Improved Switched Inductor qZSI
ESL-qZSI	Extended Switched Inductor qZSI
3P-ST	Three-phase leg ST
1P-ST	Single-phase leg ST
SBC	Simple Boost Control
MBC	Maximum Boost Control
MCBC	Maximum Constant Boost Control
ZSVM	Space Vector Modulation
CZPWM	Continuous PWM
DZPWM	Discontinuous PWM
PI	Proportional integral controller

THI	Third harmonic injection
MBDSV	Maximum boost discontinuous space vector strategy
DCPWM	Discontinuous pulse-width modulation
DZSVM2	Discontinuous Space Vector Modulation
4L-qZSI	Four-leg quasi-Z-source inverter
3DZSVM	Novel three-dimensional space vector modulation technique
VUF	Voltage unbalance factor
PLL	Phase-locked loop
DPC	Direct power controller
PWM	Pulse width modulation
MPC	Model predictive control
PDPC	Predictive direct power control
SVM	Space vector modulation
MPC	Maximum boost control
ZSVM6	Space vector modulation six *ST* duration

Electrical Variables

V_{dc}	DC-link voltage (v)
i_{L1}	Inductive current *L1* (A)
V_{C1}, V_{C2}	Capacitor voltage across C_1, C_2 (V)
e_a, e_b, e_c	Source voltage of phase a, b, c respectively (V)
V_a, V_b, V_c	Output inverter voltage of phase a, b, c respectively (V)
Sx1, *Sx2*	States for the upper and lower switch in phase (a, b, c)
D_{sh}	Shoot though duty cycle
B	Boost factor
V^*_{pv}, V_{pv}	Measured and reference PV output voltage reference (V)
V_{MPP}	Searched maximum power point voltage (V)
i_{pv}	Output PV current (A)

System Parameters:

L_1, L_2	Inductors for qZSI (H)
C_1, C_2	capacitors for qZSI (C))
M	Modulation index
ST	Shoot through
T_{sh}	Total *ST* duration (s)
T_{SW}	Switching period (s)
P&O	Perturb and observe method

K_p, k_I	Proportional and integral constants
E	Error of output PV voltage control loop
G_{PI}	Transfer function of the PI controller
p	Laplace operator
R	Resistance of the filter (Ω)
L	Inductance of the filter (H)
T_S	Sampling period (s)
P^*, q^*	Reference active and reactive power (w)
r_c, R_L	Internal resistance (Ω)
f	Line frequency (Hz)

Chapter 1

Introduction

1.1 Overview and Motivation

The limited supply of fossil fuels, being the predominant energy source, results in substantial emissions of greenhouse gases that contribute to climate change. Furthermore, the use of fossil fuels for transportation and the continued growth of industrial activities lead to significant air pollution [1], [2]. In order to alleviate these challenges, renewable energy sources (RES) have been progressively promoted as an alternative option for power generation during the past few decades, as illustrated in Figure 1.1. In 2023, the share of RES in the worldwide power generation capacity exceeded 33% [3]. The RES, in contrast to traditional fossil fuels, is environmentally beneficial as it produces energy without generating any greenhouse gases, thereby aiding in the reduction of air pollution to a certain degree.

Additionally, solar and wind energy have had substantial growth in recent years, surpassing other forms of renewable energy. This trend is illustrated in Figure 1.1, which shows that around 33% and 28% of new renewable energy installations consist of photovoltaics source (PV) and wind power, respectively

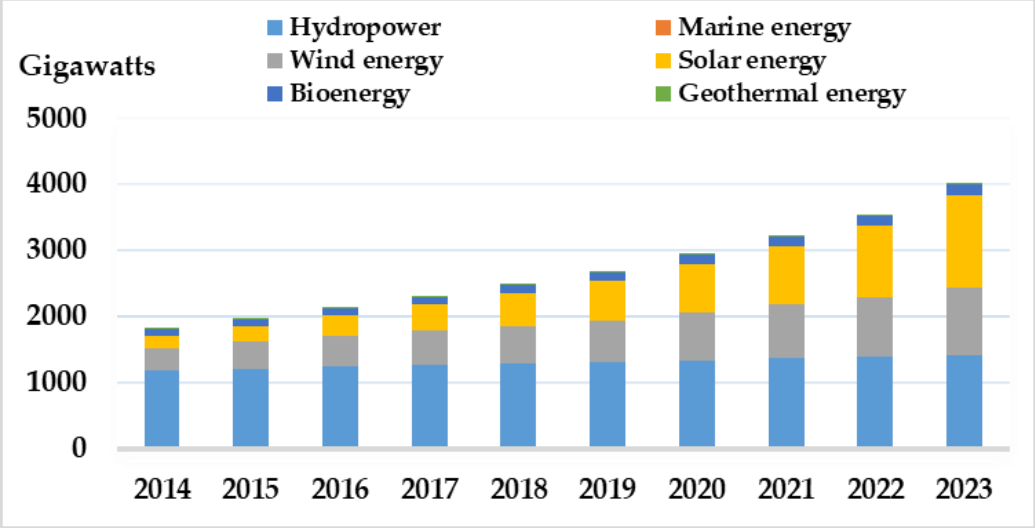


Figure 1.1 Global power generating capacity [3]

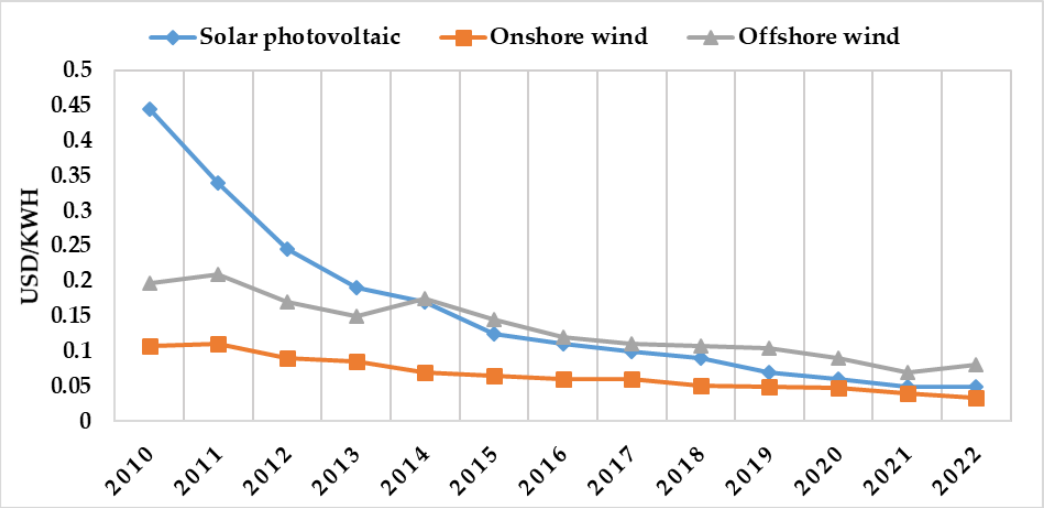


Figure 1.2 Levelised cost of electricity from newly commissioned solar PV, onshore wind power and offshore wind power, 2010-2022 [4]

The levelized cost of electricity (LCOE) for renewable energy sources has significantly decreased in recent years. Onshore wind power has seen the most dramatic drop, with the global average LCOE falling by 50% between 2010 and 2022, reaching USD 0.033/kWh. Solar PV costs have also declined, with the global average LCOE at USD 0.049/kWh in 2022. However, offshore wind remains slightly more expensive at USD 0.081/kWh (see Figure 1.2).

Despite these cost reductions, a major challenge for integrating renewable energy sources like solar PV is their intermittent nature. The DC voltage they produce fluctuates based on environmental conditions, making direct connection to the grid impractical. This has driven the development of power electronic converters (PECs) as a solution.

PECs act as interfaces between renewable energy sources and the grid. They address the challenges of fluctuating voltage by dynamically regulating it, efficiently converting power, and maintaining balanced power distribution. This ensures grid compatibility and reliable power delivery.

1.1.1 Power Electronics Converters for Renewable Energy System

The PECs play a crucial role in linking RES to the grid or load side. They have a significant influence on the system's overall operation, affecting stability, dependability, effectiveness, power quality, and consumption ratio.

In order to provide an energy conversion that is both economical and efficient, a range of innovative PEC are being created in parallel with the growing practical adoption of renewable energies [5]. Figure 1.3 illustrates a comprehensive framework for incorporating RES through the utilization of PEC. The integration of RES into the electrical system requires the utilization of PEC. In other words, PEC systems must synchronize the outputs of RES according to the power grid's requirements. Therefore, the efficiency of converters has been greatly improved. There are two ways to achieve this: *i*) by introducing new power converter designs or *ii*) by implementing improved control techniques.

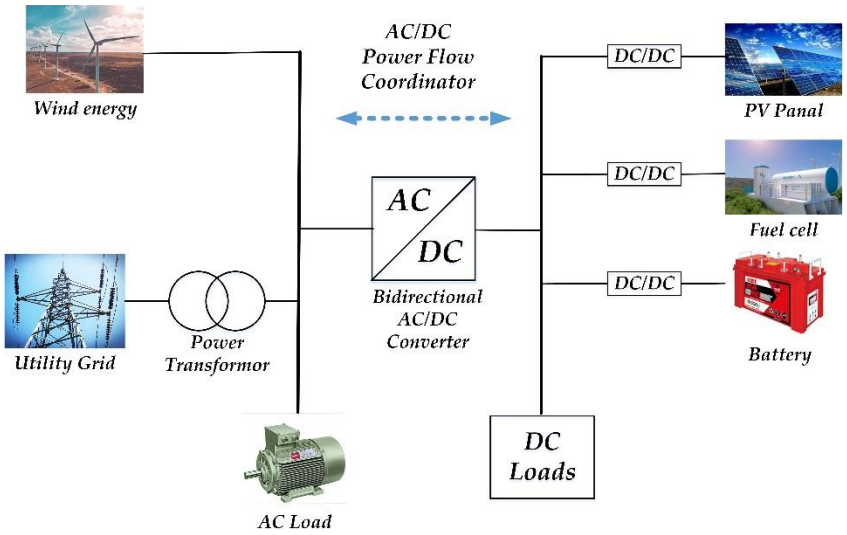


Figure 1.3 Schematic exhibiting the relationship of a RES to the electricity grid.

Moreover, the converters used in RES can be classified as galvanically isolated and non-isolated versions [6], [7]. Based on the topologies mentioned in [8], [9], [5], the isolated converters, often referred to as transformer-based converters, possess a significant potential to increase by utilizing a transformer to isolate the input and output. Nevertheless, the additional transformers may lead to increased expenses, larger dimensions, and reduced efficiency (referred to as transformer-less solutions) in comparison to their counterparts, as established by the case studies in [10], [11]. Hence, non-isolated converters exhibit higher potential in the power conversion process when considering all relevant factors.

1.1.2 Single Stage Inverter Versus Double Stage Inverter

Voltage source inverters (VSIs) are commonly utilized in a wide range of power electronics uses, including distributed power generations, battery storage, and uninterruptable power supplies (UPS) [12], [13]. Nevertheless, VSIs have certain boundaries and limitations. Which, the AC output voltage is less than the input DC voltage, which classifies them as buck converters. To increase the input DC voltage to the desired DC-link voltage, an extra DC-DC boost converter is required [14], [15]. The integration of the DC-DC boost converter enhances the complex configuration of the controller, decreases the system's overall efficacy, and raises the total price of the converter [12].

Furthermore, a dead time is also inserted between the pulses to avoid a short-circuit across the upper and lower devices. However, this dead time also leads to an increase in distortion in the output current/voltage waves [17], [18].

In order to address the limitations described above about the VSIs, impedance source inverters (ISIs) were suggested as a solution. The ISI are classified into two main subgroups based on the type of coupling in their impedance network (see Figure 1.4):

- ***Separated inductors*:** This subgroup includes the classic Z-source inverter [19], along with variations like the quasi Z-source [20], embedded Z-source

[21], improved Z-source [22], switched inductor Z-source [23], and switched inductor quasi Z-source [24]. These converters use separate inductors and capacitors in the impedance network.

- ***Magnetically coupled inductors and transformers*:** This subgroup utilizes transformers or magnetically coupled inductors to achieve specific functionalities. Examples include the Trans Z-source [25], switched coupled inductor quasi Z-source [24], Y-source [26], TZ-source [27], Γ Z-source [28], and LCCT Z-source [29].

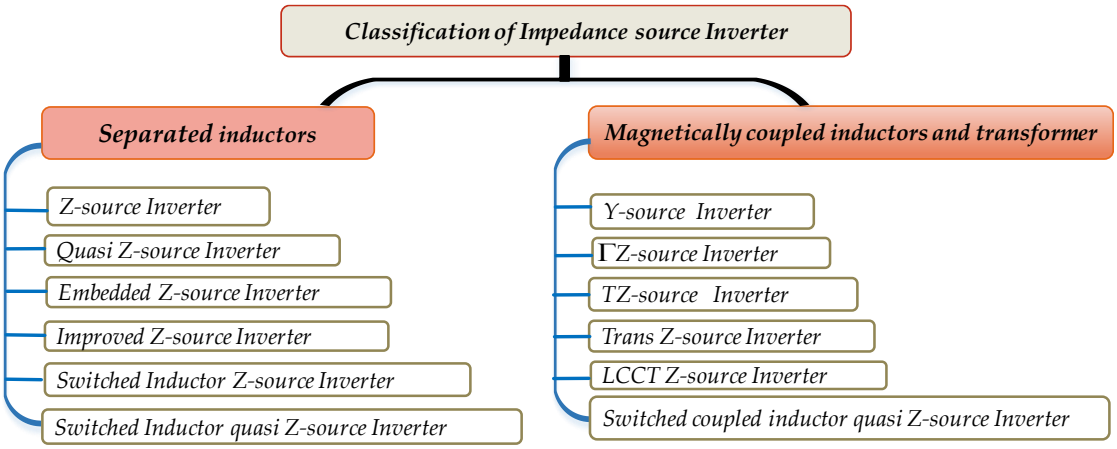


Figure 1.4 Classification of Impedance Source Networks

The initial configuration of the ISIs is the Z-source inverter (ZSI), which was introduced in 2002 as a substitute for the traditional VSI. The ZSI performs the buck-boost operation in a single-stage converter by employing a Z-source network (ZSN). This network comprises of two similar inductors, two similar capacitors, and a reverse diode [30], [31]. The ZSI can increase the input DC voltage to the required DC-link voltage by utilizing an extra switching state known as the shoot-through state (*ST)*. Consequently, the inverter's capabilities increase and its dependability is enhanced, as it remains unaffected by mis-gating caused by electromagnetic interference (EMI). The ZSI offers greater efficiency, a more simplified design, and lower costs compared to the conventional two-stage inverter, which comprises a dc-dc boost converter and a VSI [32], [33].

The quasi-Z-source inverter (qZSI) was introduced as an enhanced generation of the conventional ZSI [20]. It offers several additional benefits, including a consistent input current and the ability to connect the input DC source and DC-link bus together. Furthermore, the voltage of one of the capacitors in the quasi-Z-source network is much decreased, leading to a reduction in the size of the passive elements [34]. Considering the aforementioned features, the qZSI can be regarded as an attractive choice for many power generation systems [35]–[38]. Subsequently, other advanced configurations of ISIs have been suggested to enhance the whole performance and efficiency, as evidenced by references [32], [27–32]. However, it is possible to enhance the efficiency of the latter, the ISI circuit is naturally more complex and necessitates the use of modern and advanced control methods. A comparative

analysis, based on experimental data, is necessary to demonstrate the advantages of the qZSI over the standard two-stage inverter for power generation systems [28].

The effectiveness of ISI is reliant on the pulse-width-modulation (PWM) technique, which involves introducing the ST state in the traditional null states while preserving the active state size in order to maintain the output voltage form [41]. Several modulation algorithms were devised to regulate the three-phase ISIs. Simultaneously, the modulation schemes impose an important effect on distributing of power losses, fluctuation in current, stresses on voltage and current, and the overall efficiency of output power [42].

Various modulation techniques may be utilised to regulate the three-phase qZSI [43]. The ST state creation approach categorises specific frameworks into two categories: i) three-phase leg ST state, which includes simple boost control (SBC), maximum boost control (MBC), and maximum constant boost control (MCBC). The ST state is generated by activating the three-phase legs concurrently. ii) The single-phase leg ST prefers the space vector modulation (SVM) technique, where the ST state is achieved using only one phase-leg [44]. On the other hand, categories *i* and *ii* described previously are utilised in both continuous and discontinuous modulation schemes, specifically CZPWM and DZPWM. Among these, DZPWM is regarded as the most effective in minimising power losses [45].

Despite its wide application in several independent applications [46], the three-phase, three-leg qZSI is subject to certain limitations. An inherent limitation of this system, which was intentionally designed this way, is its ability to only accommodate symmetrical three-phase loads. Conversely, the 4L-qZSI offers many advantages such as fault tolerance, improved reliability due to the elimination of necessary dead time, and reduced trip current caused by the short circuit in each leg [47], [48].

The examination of existing literature reveals various control schemes explored for the 4L-qZSI. Among these, nonlinear controllers, specifically finite control set-model predictive control (FCS-MPC) [48]–[50], have been investigated. In contrast, space vector modulation (SVM) has demonstrated efficacy as a PWM technique. SVM stands out due to its substantial flexibility in optimizing switching waveforms and its suitability for practical implementation [51].

Commonly employed in 4L-VSI systems, three-dimensional space vector modulation (3DSVM) strategies have gained widespread usage [52]. In comparison to carrier-based PWM, 3DSVM offers several enhancements, including heightened exploitation of the dc-link and reduced output distortion.

However, it is accompanied by inherent limitations arising from the necessity for complex modeling and prolonged computational time [53]. The amalgamation of Model Predictive Control (MPC) and instantaneous power theory gives rise to a novel family of Direct Power Control (DPC) known as Predictive Direct Power Control (PDPC). In contrast to traditional DPC methods, PDPC ensures optimal vector selection by employing the power ripple minimization concept through cost function minimization [54]. Additionally, the application of Predictive Power Control with Space Vector Modulation (PDPC-SVM) is employed to mitigate the variable frequency associated with PDPC, as detailed in [55]. Furthermore, PDPC-SVM

exhibits high efficacy in harmonic current mitigation, power factor correction, and active power injection, particularly at low switching frequencies.

1.3 Dissertation Contributions

The aim of this thesis to focuses on developing advanced control strategies for Distributed Generation (DG) systems, leveraging the advantages of ZSI/qZSIs as promising types of ISIs. To achieve this goal, the research will explore the following objectives:

- To assess the ZSI/qZSI's ability to boost voltage, a comprehensive simulation-based comparison is conducted that integrates switched inductor cells. This comparison evaluates several key parameters, including voltage gain achieved, voltage stress experienced by the inverter switches, the number of active and passive components required, and the magnitude of inductive current ripple during steady-state operation.
- The comprehensive review of the various modulation strategies employed for three-phase ZSI/qZSIs. The review delves into a comparative assessment of these strategies, highlighting their advantages, limitations, and suitability for different applications.
- Introduces a new three-dimensional space vector modulation technique specifically tailored for four-leg quasi-Z-source inverters. This method is designed to enhance the overall performance of the four-leg quasi-Z-source inverters, particularly in terms of steady-state operation and reduced harmonic distortion. It achieves this by minimizing output and inductor current ripples. The proposed method demonstrably leads to lower inductor current ripples and total harmonic distortion in the output current compared to the conventional carrier-based PWM technique when both operate at the same switching frequency.
- Proposes a development of Predictive Direct Power Control for grid-tied photovoltaic systems. The proposed control method operates with a fixed switching frequency and eliminates the need for a weighting factor. It utilizes a simplified space vector modulation technique that selects the three most appropriate switching vectors for the inverter. The results demonstrate that the proposed method effectively tracks and generates the maximum power from the PV system, even with fast-changing power dynamics. Additionally, it ensures the desired AC voltage at the output and achieves superior tracking of both active and reactive power references while minimizing power ripple.

1.4 Dissertation Organization

The first chapter providing a general background on the increasing importance of renewable energy sources. It then delves into the role of power converters in integrating these renewable sources into the grid. A key focus of the chapter is a comparative analysis of single-stage and double-stage inverters, highlighting the advantages and disadvantages of each approach.

The remaining of the thesis is organized as follows:

- **Chapter 2: Impedance Source Inverters: Exploring Topologies and Control Strategies**

This chapter dives into the realm of Impedance Source Inverters (ISIs), specifically focusing on configurations that integrate switched-inductors with ZSI/qZSI. We'll analyze the strengths and weaknesses of various ZSI/qZSI topologies, equipping you to identify those that excel at boosting low DC voltage sources to high AC voltages. Additionally, the chapter explores the application of continuous conduction mode PWM (CZPWM) and discontinuous conduction mode PWM (DZPWM) for three-phase ZSI/qZSI, comparing them to a widely used modulation technique. By the chapter's conclusion, you'll be equipped with valuable insights to select the most appropriate ISI configuration and control strategy for achieving high-efficiency DC-AC

- **Chapter 3: Optimized Modulation Scheme for Four-Leg quasi Z-Source Inverter**

This chapter introduces a new three-dimensional space vector modulation technique, named 3DZSVM, specifically designed for four-leg quasi-Z-source inverters (4L-qZSI). 3DZSVM comes in three variations (3DZSVM2, 3DZSVM4, and 3DZSVM8) and aims to enhance the overall performance of the 4L-qZSI, particularly in steady-state operation and minimization of harmonic distortion. While building upon the strengths of conventional SVMs in both the *abc* and $\alpha\beta\gamma$ reference frames, 3DZSVM innovates by employing a novel $\rho\sigma\tau$ coordinate system for its design calculations. This simplification eliminates the need for trigonometric functions, streamlining the algorithm. Additionally, the method operates within a single sector, further optimizing the processes of pulse generation and time interval computations. Extensive simulations validate the effectiveness of 3DZSVM for the 4L-qZSI. Compared to conventional CZPWM methods, simulations predict significant advantages for 3DZSVM.

- **Chapter 4: Predictive Direct Power Control of qZSI for Grid-Tied PV Application**

This chapter proposes a new control method for grid-tied inverters using photovoltaic (PV) sources. The method, called simplified predictive direct power control (PDPC), aims to maximize power output from the PV system while ensuring grid stability. The PDPC uses a special model to predict power output, allowing it to operate with a constant switching frequency and avoid complex calculations. Additionally, a simplified switching technique reduces computational burden while maintaining control effectiveness. Simulations show that this PDPC effectively tracks and extracts maximum power from the PV source, even with rapidly changing conditions. It also maintains the desired AC voltage output and precisely controls both active and reactive power with minimal power fluctuations.

❖ **Chapter 5: Conclusion and Future Work**

This chapter provides a brief summary of the whole thesis and discusses some extended ideas that can be carried out in the future.

1.5 Chapter reference

[1] T. Li, A. Li, and Y. Song, "Development and utilization of renewable energy based on carbon emission reduction—evaluation of multiple MCDM methods," *Sustainability*, vol. 13, no. 17, p. 9822, 2021.

[2] M. K. G. Deshmukh, M. Sameeroddin, D. Abdul, and M. A. Sattar, "Renewable energy in the 21st century: A review," *Mater. Today Proc.*, vol. 80, pp. 1756–1759, 2023.

[3] IRENA, *Renewable Capacity Statistics 2024*. 2024. [Online]. Available: www.irena.org

[4] IRENA, *Renewable Generation Costs in 2022*. 2022.

[5] Z. Tang, Y. Yang, and F. Blaabjerg, "Power electronics: The enabling technology for renewable energy integration," *CSEE J. Power Energy Syst.*, vol. 8, no. 1, pp. 39–52, 2021.

[6] Y. P. Siwakoti, F. Z. Peng, F. Blaabjerg, P. C. Loh, and G. E. Town, "Impedance-source networks for electric power conversion part I: A topological review," *IEEE Trans. power Electron.*, vol. 30, no. 2, pp. 699–716, 2014.

[7] J. Yuan, F. Blaabjerg, Y. Yang, A. Sangwongwanich, and Y. Shen, "An overview of photovoltaic microinverters: Topology, efficiency, and reliability," in *2019 IEEE 13th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG)*, IEEE, 2019, pp. 1–6.

[8] "Applications in Photovoltaic Power Systems," in *Impedance Source Power Electronic Converters*, 2016. doi: 10.1002/9781119037088.ch14.

[9] R. Panigrahi, S. K. Mishra, S. C. Srivastava, A. K. Srivastava, and N. N. Schulz, "Grid integration of small-scale photovoltaic systems in secondary distribution network—A review," *IEEE Trans. Ind. Appl.*, vol. 56, no. 3, pp. 3178–3195, 2020.

[10] M. Islam, S. Mekhilef, and M. Hasan, "Single phase transformerless inverter topologies for grid-tied photovoltaic system: A review," *Renew. Sustain. energy Rev.*, vol. 45, pp. 69–86, 2015.

[11] D. Meneses, F. Blaabjerg, O. Garcia, and J. A. Cobos, "Review and comparison of step-up transformerless topologies for photovoltaic AC-module application," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2649–2663, 2012.

[12] J. Fang, H. Li, Y. Tang, and F. Blaabjerg, "Distributed power system virtual inertia implemented by grid-connected power converters," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8488–8499, 2017.

[13] A. Adib, B. Mirafzal, X. Wang, and F. Blaabjerg, "On stability of voltage source inverters in weak grids," *Ieee Access*, vol. 6, pp. 4427–4439, 2018.

[14] S. K. Sahoo, S. Sukchai, and F. F. Yanine, "Review and comparative study of single-stage inverters for a PV system," *Renew. Sustain. Energy Rev.*, vol. 91, pp. 962–986, 2018.

[15] J. Liu, S. Cheng, and A. Shen, "A high efficiency two-stage inverter for photovoltaic grid-connected generation systems," *J. Power Electron.*, vol. 17, no. 1, pp. 200–211, 2017.

[16] L. Chen, A. Amirahmadi, Q. Zhang, N. Kutkut, and I. Batarseh, "Design and implementation of three-phase two-stage grid-connected module integrated converter," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 3881–3892, 2013.

[17] J. W. Kolar, T. Friedli, J. Rodriguez, and P. W. Wheeler, "Review of three-phase PWM AC–AC converter topologies," *IEEE Trans. Ind. Electron.*, vol. 58, no. 11, pp. 4988–5006, 2011.

[18] J. I. Leon, S. Kouro, L. G. Franquelo, J. Rodriguez, and B. Wu, "The essential role and the continuous evolution of modulation techniques for voltage-source inverters in the past, present, and future power electronics," *IEEE Trans. Ind. Electron.*, vol. 63, no. 5, pp. 2688–2701, 2016.

[19] F. Z. Peng, "Z-source inverter," *IEEE Trans. Ind. Appl.*, vol. 39, no. 2, pp. 504–510, 2003.

[20] J. Anderson and F. Z. Peng, "Four quasi-Z-source inverters," in *2008 IEEE Power Electronics*

Specialists Conference, IEEE, 2008, pp. 2743–2749.

[21] P. C. Loh, F. Gao, and F. Blaabjerg, "Embedded EZ-source inverters," *IEEE Trans. Ind. Appl.*, vol. 46, no. 1, pp. 256–267, 2009.

[22] Y. Tang, S. Xie, and C. Zhang, "An improved $ Z $-source inverter," *IEEE Trans. power Electron.*, vol. 26, no. 12, pp. 3865–3868, 2010.

[23] M. Zhu, K. Yu, and F. L. Luo, "Switched inductor Z-source inverter," *IEEE Trans. Power Electron.*, vol. 25, no. 8, pp. 2150–2158, 2010.

[24] H. F. Ahmed, H. Cha, S.-H. Kim, and H.-G. Kim, "Switched-coupled-inductor quasi-Z-source inverter," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1241–1254, 2015.

[25] W. Qian, F. Z. Peng, and H. Cha, "Trans-Z-source inverters," *IEEE Trans. power Electron.*, vol. 26, no. 12, pp. 3453–3463, 2011.

[26] Y. P. Siwakoti, P. C. Loh, F. Blaabjerg, and G. Town, "Y-source impedance network," in *2014 IEEE applied power electronics conference and exposition-APEC 2014*, IEEE, 2014, pp. 3362–3366.

[27] M.-K. Nguyen, Y.-C. Lim, and Y.-G. Kim, "TZ-source inverters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 12, pp. 5686–5695, 2012.

[28] P. C. Loh, D. Li, and F. Blaabjerg, "Γ-Z-source inverters," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 4880–4884, 2013.

[29] M. Adamowicz, R. Strzelecki, F. Z. Peng, J. Guzinski, and H. A. Rub, "New type LCCT-Z-source inverters," in *Proceedings of the 2011 14th European Conference on Power Electronics and Applications*, IEEE, 2011, pp. 1–10.

[30] F. Z. Peng, "Z-source inverters," *Wiley Encycl. Electr. Electron. Eng.*, pp. 1–11, 1999.

[31] Y. Huang, M. Shen, F. Z. Peng, and J. Wang, "Z -Source Inverter for Residential Photovoltaic Systems," *IEEE Trans. power Electron.*, vol. 21, no. 6, pp. 1776–1782, 2006.

[32] O. Ellabban and H. Abu-Rub, "Z-source inverter: Topology improvements review," *IEEE Ind. Electron. Mag.*, vol. 10, no. 1, pp. 6–24, 2016.

[33] M. Hanif, M. Basu, and K. Gaughan, "Understanding the operation of a Z-source inverter for photovoltaic application with a design example," *IET Power Electron.*, vol. 4, no. 3, pp. 278–287, 2011.

[34] A. Battiston, J.-P. Martin, E.-H. Miliani, B. Nahid-Mobarakeh, S. Pierfederici, and F. Meibody-Tabar, "Comparison criteria for electric traction system using Z-source/quasi Z-source inverter and conventional architectures," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 2, no. 3, pp. 467–476, 2014.

[35] N. Priyadarshi, S. Padmanaban, D. M. Ionel, L. Mihet-Popa, and F. Azam, "Hybrid PV-Wind, micro-grid development using quasi-Z-source inverter modeling and control-experimental investigation," *Energies*, vol. 11, no. 9, Sep. 2018, doi: 10.3390/en11092277.

[36] A. Lashab, D. Sera, J. Martins, and J. M. Guerrero, "Dual-Input Quasi-Z-Source PV Inverter: Dynamic Modeling, Design, and Control," *IEEE Trans. Ind. Electron.*, vol. 67, no. 8, pp. 6483–6493, 2019.

[37] D. Sun *et al.*, "Modeling, impedance design, and efficiency analysis of quasi-$ Z $ source module in cascaded multilevel photovoltaic power system," *IEEE Trans. Ind. Electron.*, vol. 61, no. 11, pp. 6108–6117, 2014.

[38] A. Abid, A. Bakeer, L. Zellouma, M. Bouzidi, A. Lashab, and B. Rabhi, "Low Computational Burden Predictive Direct Power Control of Quasi Z-Source Inverter for Grid-Tied PV Applications," *Sustainability*, vol. 15, no. 5, p. 4153, 2023.

[39] N. Subhani, R. Kannan, A. Mahmud, and F. Blaabjerg, "Z-source inverter topologies with switched Z-impedance networks: A review," *IET Power Electron.*, vol. 14, no. 4, pp. 727–750, 2021.

[40] A. Abid, L. Zellouma, M. Bouzidi, A. Lashab, and B. Rabhi, "Switched Inductor Z-source/quasi Z-source Network: State of Art and Challenges," in *020 1st International Conference on Communications, Control Systems and Signal Processing (CCSSP)*, IEEE, 2020, pp. 477–482.

[41] Y. Liu, B. Ge, H. Abu-Rub, and F. Z. Peng, "Overview of space vector modulations for three-

phase Z-source/quasi-Z-source inverters," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 2098–2108, 2013.

[42] A. Abdelhakim, F. Blaabjerg, and P. Mattavelli, "Modulation schemes of the three-phase impedance source inverters—Part I: Classification and review," *IEEE Trans. Ind. Electron.*, vol. 65, no. 8, pp. 6309–6320, 2018.

[43] E. Babae, H. M. Suryawanshi, and H. Abu-Rub, "Z-source converters: topologies, modulation techniques, and applications—Part II," *IEEE Trans. Ind. Electron.*, vol. 65, no. 10, pp. 8274–8276, 2018.

[44] S. Vadi, R. Bayindir, and E. Hossain, "A review of control methods on suppression of 2ω ripple for single-phase quasi-Z-source inverter," *IEEE Access*, vol. 8, pp. 42055–42070, 2020.

[45] I. Chaib, E. M. Berkouk, J.-P. Gaubert, M. Kermadi, N. Sabeur, and S. Mekhilef, "An Improved Discontinuous Space Vector Modulation for Z-source Inverter with Reduced Power Losses," *IEEE J. Emerg. Sel. Top. Power Electron.*, 2020.

[46] Y. Li, J. Anderson, F. Z. Peng, and D. Liu, "Quasi-Z-source inverter for photovoltaic power generation systems," in *2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition*, IEEE, 2009, pp. 918–924.

[47] C. J. Gajanayake, R. Teodorescu, F. Blaabjerg, D. M. Vilathgamuwa, and P. C. Loh, "Four-leg parallel Z-source inverter based DG systems to enhance the grid performance under unbalanced conditions," in *2007 European Conference on Power Electronics and Applications*, IEEE, 2007, pp. 1–10.

[48] S. Bayhan, H. Abu-Rub, and R. S. Balog, "Model predictive control of quasi-Z-source four-leg inverter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 7, pp. 4506–4516, 2016.

[49] M. Abdelrahem, U. Degmez, R. Kennel, and J. Rodriguez, "Direct model predictive control for grid-connected four-leg quasi-z-source converter under unbalanced conditions," in *PCIM Europe digital days 2020; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, VDE, 2020, pp. 1–8.

[50] S. Bayhan, M. Trabelsi, H. Abu-Rub, and M. Malinowski, "Finite-control-set model-predictive control for a quasi-Z-source four-leg inverter under unbalanced load condition," *IEEE Trans. Ind. Electron.*, vol. 64, no. 4, pp. 2560–2569, 2016.

[51] P. Liu, J. Xu, Y. Yang, H. Wang, and F. Blaabjerg, "Impact of modulation strategies on the reliability and harmonics of impedance-source inverters," *IEEE J. Emerg. Sel. Top. Power Electron.*, 2019.

[52] R. Zhang, V. H. Prasad, D. Boroyevich, and F. C. Lee, "Three-dimensional space vector modulation for four-leg voltage-source converters," *IEEE Trans. power Electron.*, vol. 17, no. 3, pp. 314–326, 2002.

[53] J.-H. Kim and S.-K. Sul, "A carrier-based PWM method for three-phase four-leg voltage source converters," *IEEE Trans. power Electron.*, vol. 19, no. 1, pp. 66–75, 2004.

[54] M. Bouzidi, S. Barkat, A. Krama, and H. Abu-Rub, "Simplified predictive direct power control of three-phase three-level four-leg grid connected NPC converter," *IEEE Open J. Ind. Electron. Soc.*, vol. 3, pp. 448–459, 2022.

[55] A. Krama, L. Zellouma, B. Rabhi, S. S. Refaat, and M. Bouzidi, "Real-time implementation of high performance control scheme for grid-tied PV system for power quality enhancement based on MPPC-SVM optimized by PSO algorithm," *Energies*, vol. 11, no. 12, 2018, doi: 10.3390/en11123516.

Chapter 2

Impedance Source Inverters: Exploring Topologies and Control Strategies

This chapter delves into the world of Impedance Source Inverters (ISI), specifically focusing on configurations that combine switched inductors with Z-source inverter and quasi-Z-source inverters (ZSI/qZSI). We will evaluate the benefits and limitations of various ZSI/qZSI topologies, providing insights into which ones excel in boosting low DC voltage sources to high AC voltages. Additionally, the present chapter explores continuous PWM (CZPWM) and discontinuous PWM (DZPWM) for three-phase ZSI/qZSI, comparing them to a prevalent modulation technique. By the end, gain valuable insights to select the most suitable ISI configuration and control strategy for high-efficiency DC/AC conversion needs.

2.1 Overview

The ZSI has emerged as a promising topology for power electronic DC/AC converters due to its unique properties. Notably, the ZSI offers buck-boost capability and single-stage conversion, features highly desirable in various applications. The ZSI stands out for its ability to boost the input voltage using a "Shoot-Through" (*ST*) state. This not only enhances the inverter's reliability but also broadens its application potential. Compared to other power conversion systems, the ZSI offers a compelling single-stage DC/AC conversion solution with both buck and boost capabilities. Additionally, it boasts reduced cost, size, and improved efficiency due to its simpler design with fewer components. These advantages make the ZSI a highly promising and competitive topology for emerging power generation technologies like fuel cells, solar panels, and wind turbines, as well as for novel power electronics applications in areas like electric and hybrid vehicles.

2.2 Impedance Source Inverters topologies

2.2.1 Z-source Inverter

As an alternative to the conventional VSI, interest in ISIs has garnered significant attention from researchers in the field of power electronics. These inverters are recognized as single-stage buck-boost converters. The initial topology among ISIs is referred to as the Z-source inverter (ZSI), illustrated in Figure 2.1. By employing an impedance network composed of two capacitors, two inductors, and a diode, along with an additional switching state known as the shoot-through (*ST*) state, the input DC voltage can be elevated to the desired DC-link voltage. The *ST* state is activated during a portion of the zero state time [1], [2]. During the *ST* state, the output voltage remains at zero, thus not impacting the operation of the PWM inverter. While a VSI typically operates with eight switching states six active and two zero states, a ZSI features nine switching states, including six active states, two zero states, and the *ST* state. Based on the characteristics mentioned, the inverter's reliability is significantly enhanced, as the *ST* resulting from mis-gating no longer poses a risk of damaging the inverter devices. Furthermore, the Z-source network (ZSN) approach is applicable to all power conversion methods, including DC/AC, AC/DC, AC/AC, and DC/DC conversion.
The ZSI has been evaluated in various distributed generation (DG) applications, including photovoltaic (PV) systems [3]. These studies demonstrate that the one-stage ZSI effectively replaces the conventional VSI, as it can boost DC voltage as required, conduct maximum power point tracking (MPPT), and interface the PV system with the grid. Additionally, in [4] , the ZSI is employed in electric vehicle (EV) applications as a bidirectional one-stage converter, accommodating both fuel cell and battery power sources.

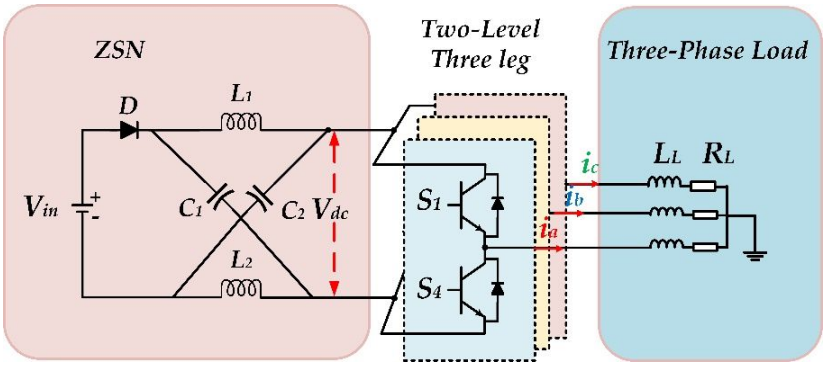


Figure 2.1: ZSI Topology

During steady-state operation, the voltages across capacitors C_1 and C_2, denoted as V_{C1} and V_{C2} respectively, can be derived as follows, assuming $C_1 = C_2$.

$$V_{C1} = V_{C2} = \frac{1 - D_{ST}}{1 - 2D_{ST}} V_{in} \tag{2.1}$$

Additionally, where D_{ST} represents the *ST* duty cycle, and V_{in} denotes the input voltage to the inverter bridge. Furthermore, the peak value of the DC-link voltage during the non-*ST* period is given by

$$V_{dc} = 2V_{C1} - V_{in} = \frac{1}{1 - 2D_{ST}} V_{in} = B.V_{in} \tag{2.2}$$

The boost factor (B) is a parameter that represents the increase in output voltage resulting from the *ST* period in the VSI. Mathematically, it is defined as $B \geq 1$. The *ST* period refers

to a short duration during which both the upper and lower switches of a leg in the inverter are simultaneously turned on, allowing the DC-link voltage to directly appear across the output phase. This period contributes to boosting the output voltage, and the boost factor quantifies this effect.

2.2.2 Quasi Z-source Inverter

The quasi Z-source inverter (qZSI) presents an alternative to the traditional ZSI, utilizing similar components in type and count (see Figure 2.2) [5]. The qZSI is particularly suited for PV systems, as it operates with continuous input current, eliminating the need for an input capacitor and thereby reducing cost and size. However, a small capacitance is often still required in practice [6].

In addition, the qZSI differs from the ZSI in that the upper capacitor operates at a lower voltage than the one below it, effectively providing only the boosted voltage. This feature distinguishes the qZSI and contributes to its suitability for various applications, especially in the context of PV systems.

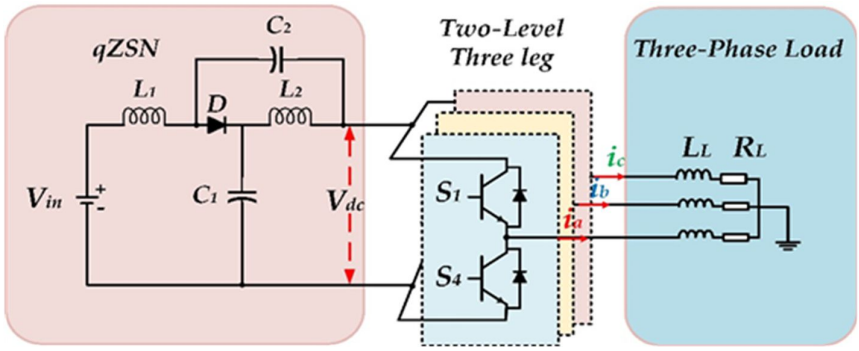
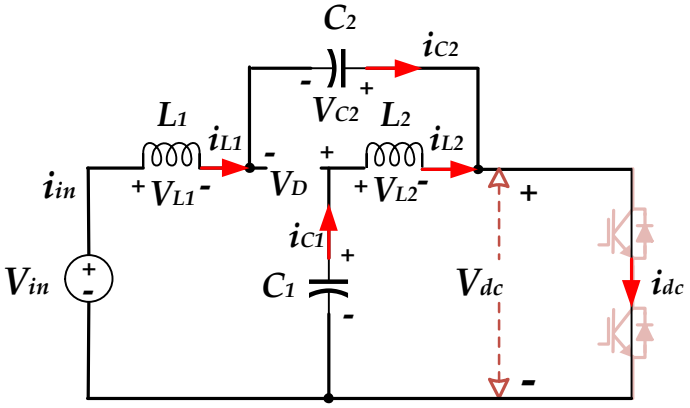
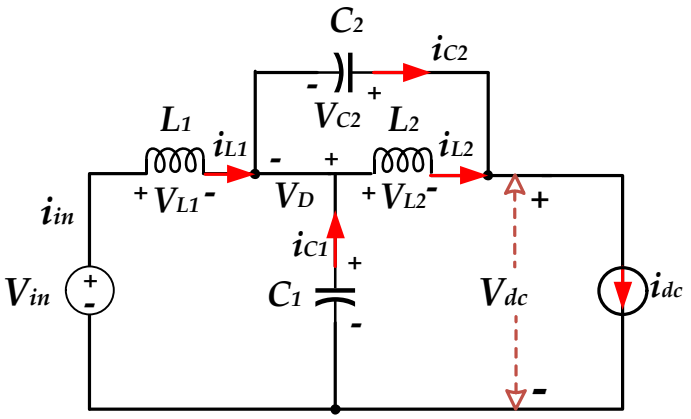


Figure 2.2: qZSI topology

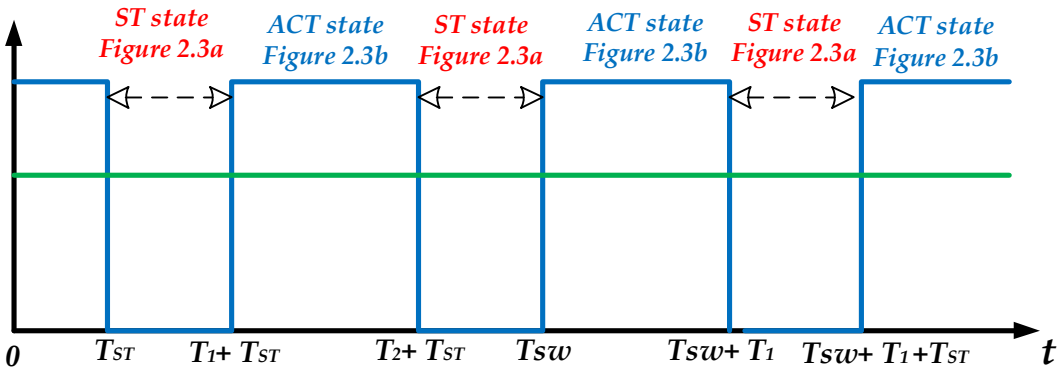
Figures 2.3(a) and 2.3(b) illustrate the circuit's two operational modes: the *ST* state and the active mode. In the *ST* state (Figure 2.3a), the DC power supply and capacitors cooperatively charge the inductors, while the diode remains off due to the reverse voltage across it. During the active mode (Figure 2.3b), the DC power supply and inductors supply energy to both the load and capacitors. The diode conducts forward current in this phase. Crucially, the *ST* duty cycle enables precise control over inductor and capacitor charging and discharging, resulting in an elevated DC voltage without necessitating an additional boost circuit [7], [5].



(a) *ST* state



(b) Active state



(c)

Figure 2.3: Equivalent qZSI circuits: (a) *ST* state, (b) Active state, (c) DC-link voltage

Considering a switching cycle with duration T_{sw} and a *ST* duration lasting T_{ST}, the remaining time within the cycle is dedicated to the active state. Therefore, $T_{sw} = T_{ST} + T_1$, and the *ST* duty ratio $D_{ST} = T_{ST} / T_{sw}$.

Figure 2.3(b) likely focuses on the specific circuit behavior during this active state interval (T_1).

$$\begin{cases} V_{L1} = V_{in} - V_{C1} \\ V_{L2} = -V_{C2} \\ V_{DC} = V_{C1} - V_{L2} = V_{C1} + V_{C2} \\ V_D = 0 \end{cases} \tag{2.3}$$

During the interval of the *ST* state, Figure 2.3(a) provides the following details:

$$\begin{cases} V_{L1} = V_{in} + V_{L2} \\ V_{L2} = V_{C2} \\ V_{dc} = 0 \\ V_D = -(V_{C1} + V_{C2}) \end{cases} \tag{2.4}$$

The inductors' average voltage during a single switching cycle is zero in steady state. According to (2.3) and (2.4), we have

$$\begin{cases} V_{L1} = \overline{V_{L1}} = \dfrac{T_{ST}(V_{C1} + V_{in}) + T_1(V_{in} - V_{C1})}{T_{sw}} \\ V_{L2} = \overline{V_{L2}} = \dfrac{T_{ST}(V_{C1}) + T_1(-V_{C2})}{T_{sw}} \end{cases} \tag{2.5}$$

During steady state conditions, the capacitor voltages and the peak DC-link voltage across the inverter bridge can be determined as follows:

$$V_{C1} = \frac{1 - D_{ST}}{1 - 2D_{ST}} V_{in}, V_{C2} = \frac{D_{ST}}{1 - 2D_{ST}} V_{in} \tag{2.6}$$

$$V_{dc} = V_{C1} + V_{C2} = \frac{1}{1 - 2D_{ST}} V_{in} = B.V_{in} \tag{2.7}$$

where B is the qZSI's boost factor. Figure 2.3c illustrates the DC-link voltage, which exhibits pulsating behavior. In the steady state, the DC-link voltage reaches a zero value. During the active state, the voltage reaches its peak value. It is possible to determine the average currents of the inductors L_1 and L_2 by using the system power rating (P).

$$i_{L1} = i_{L2} = i_{in} = P / V_{in} \tag{2.8}$$

Using Kirchhoff's current laws, we have

$$\begin{cases} i_{C1} = i_{C2} = i_{dc} - i_{L1} \\ i_D = 2i_{L1} - i_{DC} \end{cases} \tag{2.9}$$

In summary, Table 2.1 presents the voltage and current stress of the both ZSI/qZSI. Where M is the modulation index, $m = (1\text{-}D_{ST})/(1\text{-}2D_{ST})$, $n = D_{ST}/(1\text{-}2D_{ST})$, $B = 1/(1\text{-}2D_{ST})$. The Calculation of the peak output AC voltage of the qZSI is possible through the following equation

$$V_{AC} = B.M.\frac{V_{in}}{2} \tag{2.10}$$

From Table 2.1 we can demonstrate that the qZSI shares all the benefits of the ZSI, including the ability to adjust voltage up or down (buck or boost), handle a wide range of input voltages, and deliver the precise voltage needed for the load or grid connection, all in a single stage. This single-stage operation reduces the number of switches required in the PV system, leading to lower cost and improved overall efficiency. The qZSI tackles low PV panel voltage by boosting the DC-link voltage, eliminating the need for extra panels to achieve higher DC voltage or oversizing the inverter [8]. Additionally, its ability to handle the *ST* state enhances its reliability compared to conventional VSIs. This characteristic also allows the control schemes to operate without dead time, minimizing output distortion.

In addition, the qZSI offers distinct advantages over traditional ZSIs [5]. Notably, while the ZSI experiences a discontinuous input current during boost mode, the qZSI maintains a continuous input current thanks to the presence of the input inductor L_1.

This significantly reduces input stress, allowing for a reduction in the capacitance required at the output of the PV panels. While both capacitors in the ZSI experience the same high voltage, the voltage on capacitor C_2 in the qZSI is maintained at a lower level, allowing for a lower capacitor voltage rating. Additionally, in the qZSI, a common DC rail exists between the source and the inverter. This configuration facilitates easier assembly and minimizes EMI issues.

Table 2.1 Voltage and current characteristics of both ZSI/qZSI

	$V_{L1}=V_{L2}$		V_{dc}		V_D		V_{C1}	V_{C2}	V_{AC}	$i_{in}=i_{L1}=i_{L2}$	$i_{C1}=i_{C2}$	i_D
Time	T_{ST}	T_1	T_{ST}	T_1	T_{ST}	T_1	T_{ST}, T_1	T_{ST}, T_1	T_{ST}, T_1	T_{ST}, T_1	T_{ST}, T_1	T_{ST}, T_1
ZSI	mV_{in}	$-nV_{in}$	0	BV_{in}	BV_{in}	0	mV_{in}	mV_{in}	$MBV_{in}/2$	P/V_{in}	$i_{dc}-i_{L1}$	$2i_{L1}-i_{dc}$
qZSI	mV_{in}	$-nV_{in}$	0	BV_{in}	BV_{in}	0	mV_{in}	nV_{in}	$MBV_{in}/2$	P/V_{in}	$i_{dc}-i_{L1}$	$2i_{L1}-i_{dc}$

2.2.3 Switched Inductor Z-Source Inverter

To enhance the boosting capability of the ZSI, the concept of the switched inductor (SL) technique is incorporated into the ZSI. The two inductors are replaced by two SL cells, enabling the generation of a higher DC-link voltage for the main power circuit from a low input DC voltage [9]. Figure. 2.4 illustrates the switched inductor Z-source inverter (SL-ZSI). In the steady state, the average capacitor and DC-link voltages are defined by:

$$V_{C1} = V_{C2} = \frac{1-D_{ST}}{1-3D_{ST}} V_{in} \tag{2.11}$$

$$V_{dc} = V_{C1} + V_{C2} = \frac{1+D_{ST}}{1-3D_{ST}} V_{in} \tag{2.12}$$

From (2.11) and (2.12), it is evident that the boost factor is significantly increased, and the capacitor voltage is smaller compared to the ZSI. This indicates that a higher voltage gain can be achieved by using a shorter time for the *ST* state. However, the main disadvantages of this topology are the discontinuous DC input current and the inrush current at startup [10].

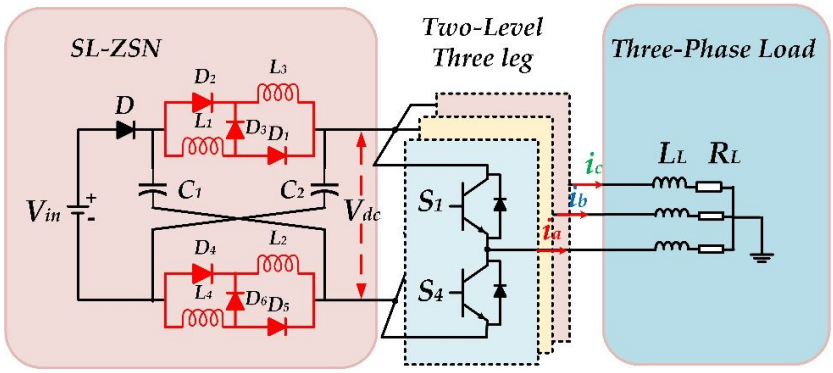


Figure 2.4: SL-ZSI topology

2.2.4 Switched Inductor Quasi Z-Source Inverter

The switched inductor quasi Z-source inverter (SL-qZSI) is introduced in [11]. To address the limitations of the boost factor in the qZSI and the discontinuous DC input current of the SL-ZSI, the SL cell is replaced by the output side inductor L_2. This cell comprises two inductors (L_2, L_3) and three diodes (D_1, D_2, D_3), as depicted in Figure 2.5. In the steady state, the following equations are valid:

$$V_{C1} = \frac{1-D_{ST}}{1-2D_{ST}+D_{ST}^2} V_{in}, \; V_{C2} = \frac{2D_{ST}}{1-2D_{ST}+D_{ST}^2} V_{in} \tag{2.13}$$

$$V_{dc} = V_{C1} + V_{C2} = \frac{1+D_{ST}}{1-2D_{ST}+D_{ST}^2} \tag{2.14}$$

As evident from (2.13) and (2.14), the boost voltage capability of the SL-qZSI surpasses that of the ZSI but lower than the SL-ZSI. However, the voltage stress on the capacitors is reduced. This topology finds application in fuel cells or renewable sources scenarios, where it efficiently converts a low input voltage into a significantly higher output voltage [12].

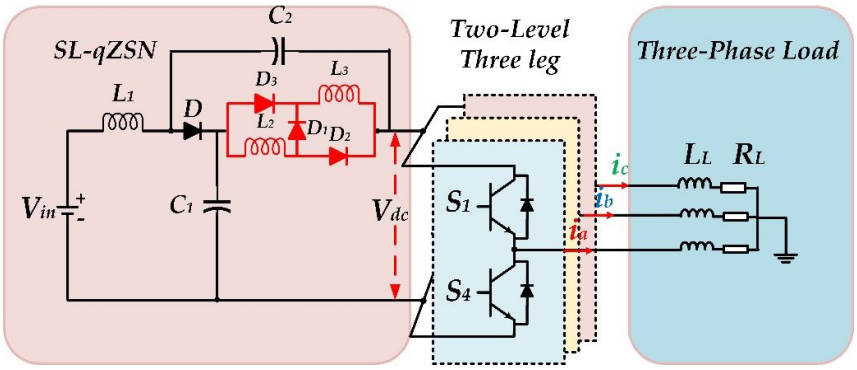


Figure 2.5: SL-qZSI topology

2.2.5 Voltage Lifting Switched Inductor Quasi Z-Source Inverter

To enhance the boosting capability while retaining all the advantages of the SL-qZSI, one of the diodes in the SL unit can be replaced by a capacitor, as depicted in Figure 2.6. For the same input and output voltage, the voltage lifting switched inductor quasi Z-source Inverter (VL-SL-qZSI) significantly reduces the *ST* duration. This advantage reduces conduction loss during the *ST* state, ultimately improving efficiency [13], [14]. In the steady state, the average voltages of capacitors and the DC-link can be assessed as follows:

$$V_{C1} = V_{VL} = \frac{1-D_{ST}}{1-3D_{ST}} V_{in},\ V_{C2} = \frac{1+D_{ST}}{1-3D_{ST}} V_{in} \tag{2.15}$$

$$V_{dc} = \frac{2}{1-3D_{ST}} V_{in} \tag{2.16}$$

According to (2.16), and compared to the ZSI and SL-qZSI, the VL-SL-qZSI can achieve a high voltage conversion ratio when the *ST* duty ratio ($0 \le D_{ST} \le 1/3$). Therefore, it is well-suited for low voltage and low power applications [15].

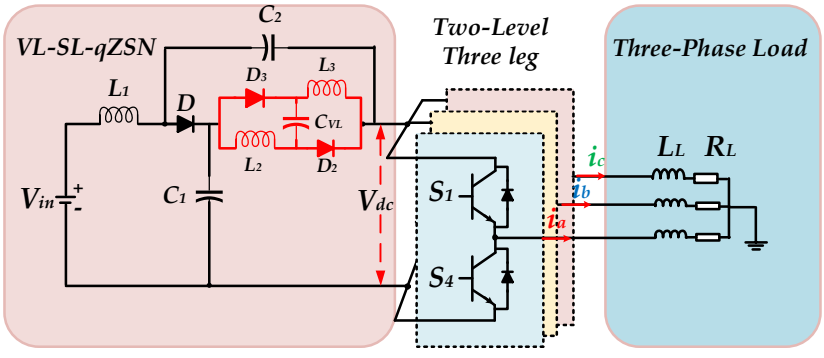


Figure 2.6: VL-SL-qZSI Topologie.

2.2.6 Switched Coupled Inductor quasi Z-Source Inverter

Recently, coupled inductors based impedance networks have been introduced to address the limitations of the qZSI's boost ability, higher voltage stresses in elements, and low output power quality. These networks provide a higher boost factor, a short *ST* time, and decrease the number and dimensions of passive elements [16]. The switched coupled inductor quasi Z-source inverter (SCL-qZSI) is presented in reference [17]. The design includes a three-winding switched coupled inductor (SCL) and switched capacitor in the conventional qZSI.

Figure 2.7 depicts the SCL-qZSI, which retains the benefits of the qZSI design, including constant input current, a shared ground between the main circuit and DC voltage source, and reduction of start inrush current [18]. Under equilibrium conditions, the following relationships are established:

$$V_{C1}=\frac{1-D_{ST}}{n+2}V_{in},\ V_{C2}=\frac{n+1+D_{ST}}{n+2}V_{in},\ V_{C2}=\frac{n+1}{(1-(3+n)D_{ST})}V_{in} \tag{2.17}$$

When the turn n=1

$$V_{dc}=\frac{3}{1-4D_{ST}}V_{in} \tag{2.18}$$

The SCL comprises three windings: N_1, N_2, and N_3. Winding N_1 and N_2 have an equal number of turns ($N_1 = N_2$) and the turn ratio of winding N_3 to N_1 (or N_2) is n ($n = N_3/N_1 = N_3/N_2$). This architecture provides increased step-up advantages by allowing winding turn ratios as low as unity (n=1). The voltage increase it provides is greater than that of the qZSI.

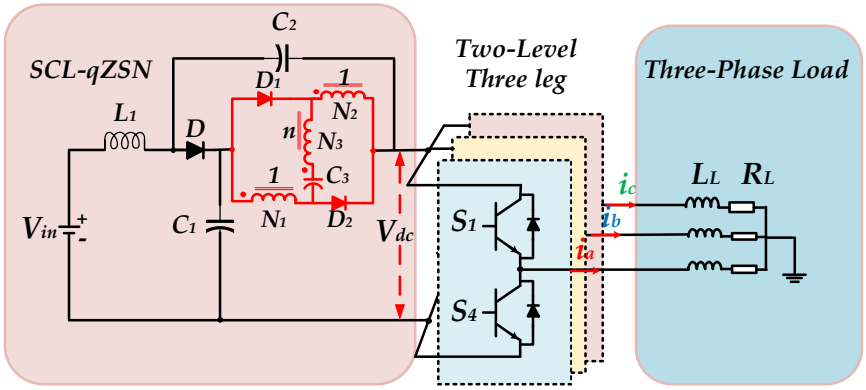


Figure 2.7: SCL-qZSI Topology

2.2.7 Ripple Switched inductor quasi Z-source Inverter

Figure 2.8 illustrates the ripple switched inductor quasi Z-source inverter (rSL-qZSI). This design addresses the challenge of startup inrush current in the SL-qZSI by replacing the two original inductors (L_1, L_2) with two cells SL within the conventional qZSI. This modification offers the advantage of reduced voltage stress on the capacitors, thereby enhancing the overall reliability of the system, as documented in [19], [20].

$$V_{C1}=\frac{1-D_{ST}}{1-3D_{ST}}V_{in},\ V_{C2}=\frac{2D_{ST}}{1-3D_{ST}}V_{in} \tag{2.19}$$

$$V_{dc}=V_{C1}+V_{C2}=\frac{1+D_{ST}}{1-3D_{ST}}V_{in} \tag{2.20}$$

A comparison of equations (2.12) and (2.20) reveals that the rSL-qZSI design achieves a boost factor equivalent to that of the SL-ZSI, while simultaneously experiencing lower voltage stress on its capacitors. This characteristic renders the rSL-qZSI particularly well-suited for applications involving low and medium power photovoltaic or fuel cell energy generation.

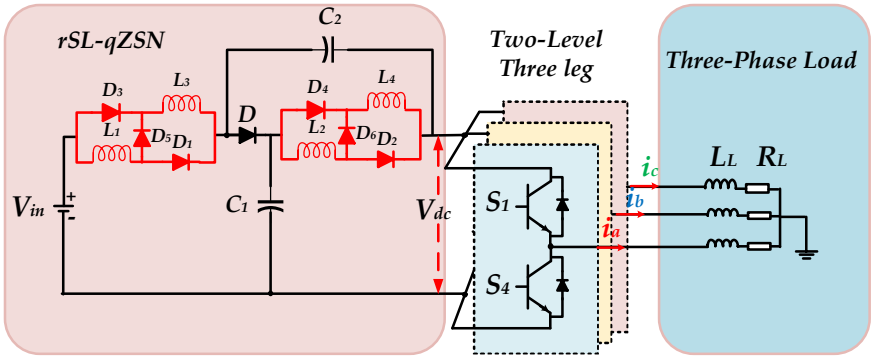


Figure 2.8: rSL-qZSI Topology

2.2.8 Switched Inductor quasi Z-source Network with Continuous Input Current

In the quest to improve the conventional qZSI topology, researchers have incorporated a switched inductor cell as a substitute for the two main inductors. This novel approach, termed the continuous input current switched inductor quasi-Z-source inverter (cSL-qZSI), is depicted in Figure 2.9. In a steady-state operating condition, the following relationships hold true [19]:

$$V_{C1} = \frac{1-D_{ST}}{(1+D_{ST})(1-3D_{ST})}V_{in},\quad V_{C2} = \frac{2D_{ST}}{(1+D_{ST})(1-3D_{ST})}V_{in} \tag{2.21}$$

$$V_{dc} = \frac{1}{1-D_{ST}}V_{in} \tag{2.22}$$

Compared to (2.12) for the SL-ZSI, and (2.22) demonstrates that the cSL-qZSI offers a lower boost factor. This translates to reduced voltage stress on the capacitors, enhancing their lifespan. Additionally, the cSL-qZSI exhibits soft-start behavior by limiting the inrush current during startup, further improving the overall lifetime of the devices [20].

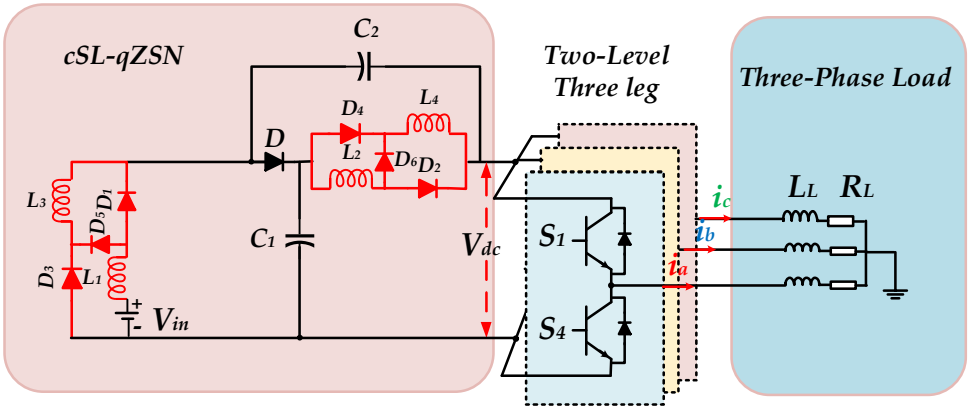


Figure 2.9: cSL-qZSI Topology

2.2.9 Switched Inductor-Improved Switched Inductor quasi Z-source Inverter

Building upon the benefits of the qZSI, the switched inductor and improved switched inductor qZSI (SL-ISL-qZSI) inherits the common ground between the DC input and output, while offering enhanced boosting capability and reduced voltage stress on the switches [21]. These improvements contribute to increased reliability and efficiency of the SL-ISL-qZSI. Figure 2.10 depicts the configuration of the SL-ISL-qZSI, achieved by replacing the main inductors (L_1, L_2) of the qZSI with the SL cell and ISL cell, respectively. The final derivations for the voltages across the capacitors and the DC-link voltage are presented as follows.

$$V_{C1} = V_{C3} = \frac{1-D_{ST}^2}{1-4D_{ST}-D_{ST}^2} V_{in}, \quad V_{C2} = \frac{(1+D_{ST})^2}{1-4D_{ST}-D_{ST}^2} V_{in} \tag{2.23}$$

$$V_{dc} = V_{C1} + V_{C3} = \frac{1-2D_{ST}}{1-4D_{ST}-D_{ST}^2} V_{in} \tag{2.24}$$

Compared to other inverter operating under identical *ST* duty cycles, the SL-ISL-qZSI achieves the highest boost factor, as evidenced by (2.23) and (2.24), despite having the same total component count. This attribute makes it particularly suitable for applications demanding high voltage conversion gain, such as photovoltaic power generation systems.

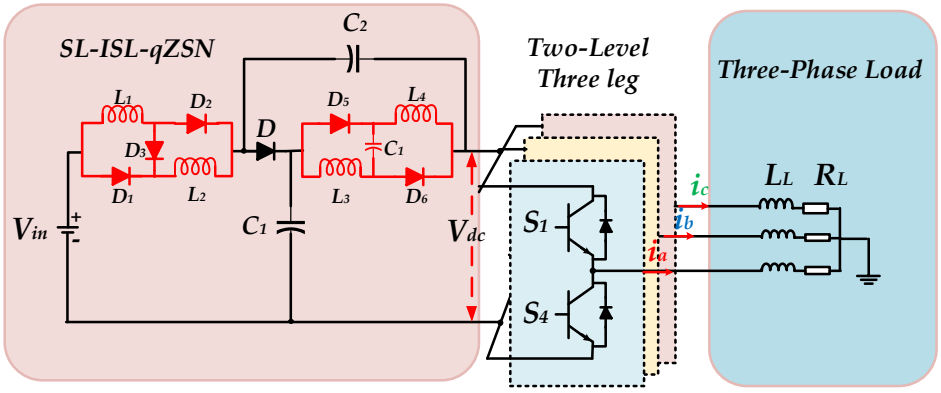


Figure 2.10. SL-ISL-qZSI Topology

2.2.10 Extended Switched inductor quasi Z-source Inverter

Figure 2.11 illustrates the extended switched inductor qZSI (ESL-qZSI), a topology designed for enhanced voltage boosting. It merges the SL-qZSI with a traditional boost DC/DC converter while incorporating an improved SL cell, replacing the original output-side inductor [22], [23]. Despite an increase in components, the ESL-qZSI achieves a superior boost capability when compared to other topologies operating under the same *ST* duty cycle. Notably, for equivalent input and output voltages, the ESL-qZSI experiences lower voltage stress across its capacitors, diodes, and switches, potentially improving the network's overall reliability. The mathematical expressions for the voltages across the capacitors and the DC-link voltage are presented as follows.

$$V_{C1}=\frac{2D_{ST}}{(1-3D_{ST})(1-D_{ST})}V_{in},V_{C2}=\frac{1+D_{ST}}{(1-3D_{ST})(1-D_{ST})}V_{in}$$
$$V_{C3}=\frac{1}{1-D_{ST}}V_{in},\qquad V_{C4}=\frac{1-D_{ST}}{(1-3D_{ST})(1-D_{ST})}V_{in} \tag{2.25}$$

$$V_{dc}=V_{C1}+V_{C2}+V_{C3}=\frac{2}{(1-3D_{ST})(1-D_{ST})}V_{in} \tag{2.26}$$

Leveraging its ability to achieve high voltage gain with continuous input current alongside reduced voltage stress across its capacitors, the ESL-qZSI emerges as a compelling candidate for distributed generation applications utilizing low-voltage input sources, such as fuel cells and photovoltaic systems.

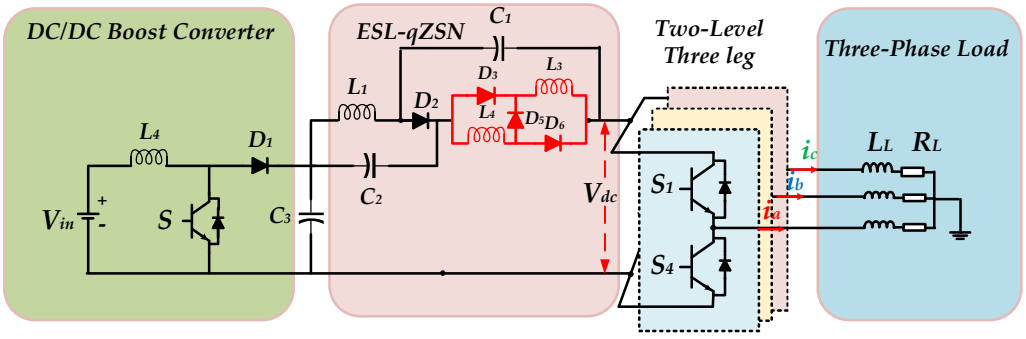


Figure 2.11. ESL-qZSI Topology

2.3 Comparative analysis

Figure 2.12 illustrates the relationship between the boost factor and the *ST* duty cycle for these various topologies. Despite having a similar component count, the SL-ZSI and rSL-qZSI topologies offer the same boost capability, while the cSL-qZSI achieves a slightly lower boost factor. However, the SL-ZSI exhibits a discontinuous input current, whereas the rSL-qZSI features a continuous input current with some ripple. Table 2.2 presents different characteristics of the formerly discussed inverters.

Table 2.2 Characteristics of different switched inductor Z-source/quasi Z-source combinations

Converter	No. of elements	Boost Factor	Continuous input Current	Startup inrush Current	Common Earth	Application
DC-DC Boost	1Capacitor 1 Inductor 1 Diode 1 Switch	$\frac{1}{1-D_{ST}}$ Where $0<D_{ST}<1$	Yes	No	Yes	/
ZSI	2 Capacitors 2 Inductors 1 Diode	$\frac{1}{1-2D_{ST}}$ Where $0<D_{ST}<1/2$	No	Yes	No	Hybrid PV-Wind [24]
qZSI	2 Capacitors 2 Inductors 1 Diode	$\frac{1}{1-2D_{ST}}$ Where $0<D_{ST}<1/2$	Yes	No	Yes	PV [25] Electric vehicles [26]
SL-ZSI	2 Capacitors 4 Inductors 7 Diode	$\frac{1+D_{ST}}{1-3D_{ST}}$ Where $0<D_{ST}<1/3$	No	Yes	No	PV System [27]

SL-qZSI	2 Capacitors 3 Inductors 4 Diode	$\frac{1+D_{ST}}{1-2D_{ST}-D_{ST}^2}$ Where $0 < D_{ST} < 1/2$	Yes	No	Yes	PV system[28] Wind system [29]
VL-SL-qZSI	3 Capacitors 3 Inductors 3 Diode	$\frac{2}{1-3D_{ST}}$ Where $0 < D_{ST} < 1/3$	Yes	No	Yes	PV system [30]
SCL-qZSI	1 Coupled inductor 3 Capacitors 1 Inductors 3 Diode	$\frac{2}{1-4D_{ST}}$ For $n = 1$, Where $0 < D_{ST} < 1/4$	Yes	No	Yes	/
rSL-qZSI	2 Capacitors 4 Inductors 7 Diode	$\frac{1+D_{ST}}{1-3D_{ST}}$ Where $0 < D_{ST} < 1/3$	Yes, rippled	No	Yes	/
cSL-qZSI	2 Capacitors 4 Inductors 7 Diode	$\frac{1}{1-3D_{ST}}$ Where $0 < D_{ST} < 1/3$	Yes	No	Yes	/
SL-ISL-qZSI	3 Capacitors 4 Inductors 5 Diode	$\frac{2(1+D_{ST})}{1-4D_{ST}-D_{ST}^2}$ Where $0 < D_{ST} < \sqrt{5}-2$	Yes	No	Yes	/
ESL-qZSI	4 Capacitors 4 Inductors 1 Switch 5 Diode	$\frac{2}{(1-3D_{ST})(1-D_{ST})}$ Where $0 < D_{ST} < 1/3$	Yes	No	Yes	/

Therefore, for *ST* duty ratios below ($\sqrt{5}$-2), the SL-ISL-qZSI topology is preferable due to its superior boost factor. Conversely, the ESL-qZSI topology offers a higher boost factor at a lower shoot-through duty cycle of $0<D_{ST}<1/3$. Notably, both the SL-qZSI and SCL-qZSI topologies boast a lower component count compared to the previously discussed ones.

Among the ZSI family topologies, the SL-qZSI exhibits the lowest boost factor, yet it remains higher than that of the classical ZSI topology. Conversely, the SCL-qZSI topology achieves the highest boost factor by employing a magnetically coupled inductor. Consequently, the SL-ISL-qZSI topology emerges as a strong candidate, particularly when prioritizing a high boost factor, a small *ST* duty cycle, a lower component count, continuous input current, common earthing, and superior efficiency.

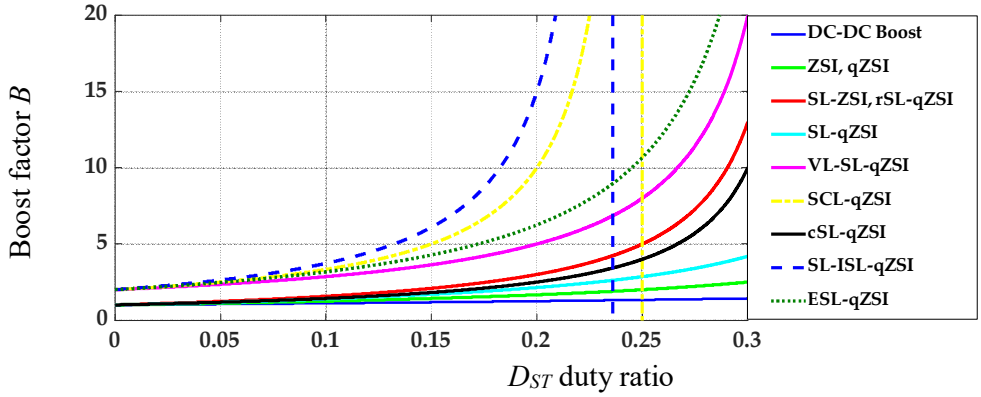


Figure 2.12: Relationship between the boost factor *B* and the D_{ST} duty cycle for different inverters

2.4 Advantages and disadvantages of the main ISI topologies

Main ISI-based SL cell topologies offer both advantages and disadvantages, which are detailed in Table 2.3. Among these ISI topologies, the qZSI architecture stands out as particularly promising for applications involving multi-source renewable energy.

Table 2.3: Summary of the ISI topologies advantages and disadvantages

Converter	Advantages	Disadvantages
ZSI	▪ Overcomes the disadvantages of VSI ▪ Inductor of current fed ZSI sustains high current. ▪ Benefits to motor drives and renewable energy generation applications.	▪ Cannot suppress the inrush current. ▪ Different grounds for source and inverter circuits ▪ High voltage capacitors which are required increase the cost and volume of the system.
qZSI	▪ Continuous input current. ▪ Reduces passive component ratings. ▪ Provides lower current stress on inductors compared to ZSI. ▪ Shares common ground with input DC supply	▪ The shoot through duty ratio always be less than 0.5. ▪ Not suitable for very low input DC voltage.
SL-ZSI	▪ Higher voltage boost capability than ZSI. ▪ Improved output power quality due to shorter D_{ST} state. ▪ Maintains buck-boost functionality like ZSI.	▪ Increased circuit complexity compared to ZSI. ▪ Uneven stress distribution on components. ▪ Limited performance at low input DC voltages. ▪ Potentially larger size and higher cost.
SL-qZSI	▪ Achieves greater output voltage increase from the DC source compared to a qZSI. ▪ lower voltage stress on capacitors compared to a ZSI. ▪ Continuous Input Current ▪ higher efficiency due to better control and reduced component stress.	▪ More complex circuit design and control strategy compared to a QZSI. ▪ Requires careful design to avoid potential *ST* current faults. ▪ Additional components can lead to a larger footprint and potentially higher cost.
VL-SL-qZSI	▪ Achieves a higher voltage boost from the DC source compared to a standard qZSI. ▪ Potentially reduces voltage stress on capacitors, improving reliability compared to a ZSI. ▪ Maintains a more continuous input current for the DC power source. ▪ Holds potential for higher efficiency due to better control over the power flow.	▪ The addition of a SL network increases the complexity of the circuit design and control strategy. ▪ Improper control can lead to *ST* current, a serious fault condition. ▪ Have low input DC voltages, experiencing issues with maintaining continuous current and inrush current at startup.
SCL-qZSI	▪ Achieves a higher boost in output voltage compared to a standard qZSI ▪ The design can potentially reduce voltage stress on its capacitors compared to a traditional ZSI. ▪ With better control over the power flow and potentially reduced component stress, the SL-qZSI might offer higher efficiency than some ZSI variants.	▪ The SCL network significantly increases the complexity of the circuit design and control strategy compared to a simpler qZSI. ▪ Careful design and control are crucial to avoid potential ST current, a fault condition that can damage the inverter. ▪ The additional components can contribute to a larger footprint and potentially higher cost compared to simpler inverters.
rSL-qZSI	▪ Addresses the challenge of startup inrush current in the SL-qZSI ▪ Reduced voltage stress on the capacitors, thereby enhancing the overall reliability of the system ▪ Achieves a boost factor equivalent to that of the SL-ZSI	▪ The design requires two capacitors that can handle significantly higher voltage compared to other components in the circuit ▪ The DC voltage gain is less
cSL-qZSI	▪ The input current is continuous ▪ Exhibits soft-start behavior by limiting the inrush current during startup	▪ The design requires two capacitors that can handle significantly higher voltage compared to other components in the circuit

	▪ Suitable for renewable energy generation.	▪ The DC voltage gain is less
SL-ISL-qZSI	▪ Inherits the common ground between the DC input and output ▪ Enhanced boosting capability and reduced voltage stress on the switches.	▪ Not suitable for very low input DC voltages
ESL-qZSI	▪ Achieves a superior boost capability when compared to other topologies operating under the same shoot-through duty cycle. ▪ Lower voltage stress across its capacitors, diodes, and switches	▪ The switched inductor network significantly increases the complexity of the circuit design ▪ Very low input DC voltages. It might struggle with maintaining continuous input current and experience inrush current issues at startup.

2.5 Pulse Width Modulation Techniques

The effectiveness of the ISI is influenced by the chosen Pulse-Width Modulation (PWM) technique. This technique involves strategically placing *ST* states within the usual null states of the output voltage waveform. Importantly, the duration of the active states remains unchanged, ensuring the overall voltage profile is maintained. Various modulation techniques are being developed to control three-phase ISI. These techniques significantly impact several key aspects of ISI operation. They influence how power losses are distributed, the amount of current ripple that occurs, the stress that is placed on voltage and current, and ultimately, the quality of the power that is delivered to the output.

Multiple modulation techniques exist to control three-phase qZSI. As shown in Figure 2.13 of reference [31]. The method used to create the ST state divides modulation techniques into two categories:

- **Three-phase leg *ST* (3P-*ST*) state**: In this approach, the ST state is generated simultaneously across all three phases of the inverter. Examples include Simple Boost Control (SBC), Maximum Boost Control (MBC), and Maximum Constant Boost Control (MCBC).
- **Single-phase leg *ST* (1P-*ST*) state**: This method utilizes a strategy like Space Vector Modulation (ZSVM) to create the *ST* state through only one phase leg at a time.

Furthermore, both categories (three-phase and single-phase) can be implemented using either continuous or discontinuous modulation schemes:

- **Continuous PWM (CZPWM):** This scheme can be worked under all of the number of switching transitions for the qZSI.
- **Discontinuous PWM (DZPWM):** reduces the switching losses in the inverter bridge by strategically switching only two of the three phases at a time. This approach minimizes the number of switching transitions compared to methods that switch all three phases simultaneously.

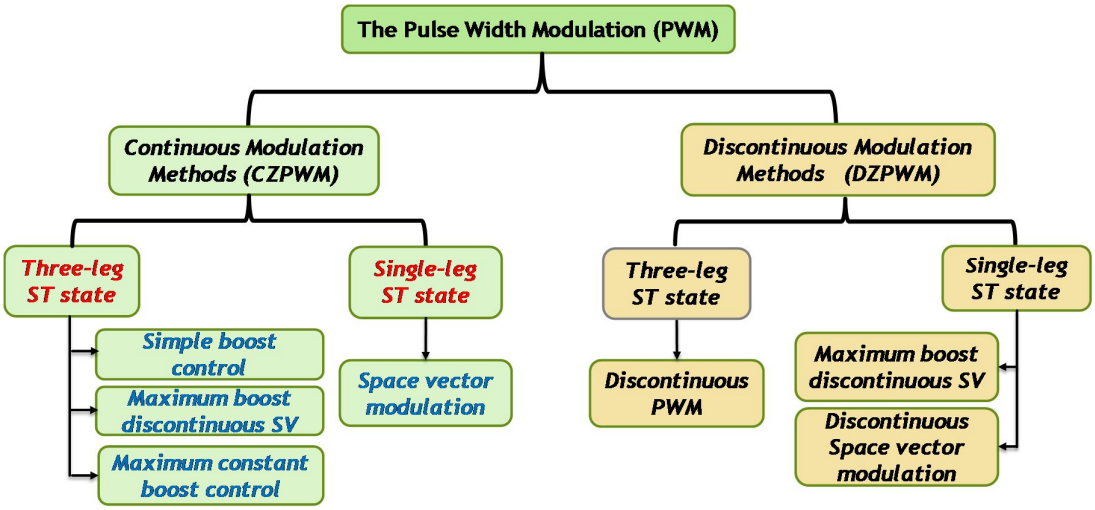


Figure 2.13 The classification of the PWM for qZSI

2.5.1 Continuous PWM

2.5.1.1 Simple Boost Control

The simple boost control (SBC) method introduces *ST* states by using two strategically placed lines (V_p and V_n) within the regular switching pattern (see Figure 2.14). The triangular carrier waveform (V_r) is compared to these lines to determine the *ST* intervals. When the carrier goes above V_p or below V_n, the inverter switches enter a *ST* state. During all other times, the inverter operates with standard active and zero states [2].

This approach offers a crucial benefit: a constant *ST* time per switching cycle, which translates to a consistent boost factor. However, there's a trade-off. As the modulation index (M) increases, the achievable *ST* duty ratio in SBC actually decreases.

SBPWM keeps the boost factor constant by using *ST* states. However, the amount of *ST* duty ratio can't exceed (1 - M). As you increase M, the *ST* duty ratio goes down to zero. At that point, the inverter behaves just like a regular VSI with no *ST*. On the plus side, SBC eliminates output frequency ripple in the DC current and voltage.

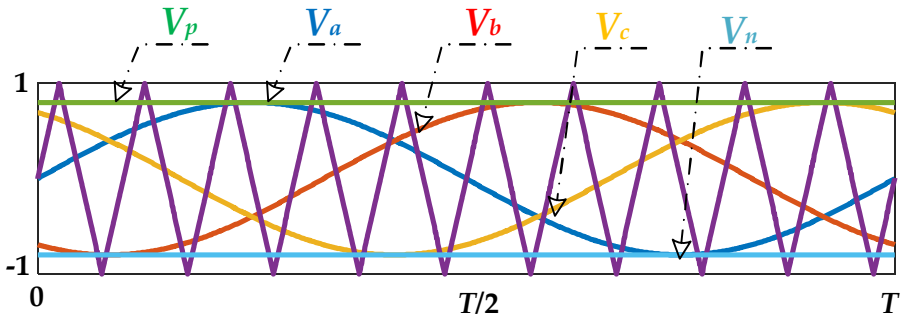


Figure 2.14: Simple boost control method

2.5.1.2 Maximum Boost Control

In Maximum Boost control (MBC) method, the *ST* reference is set to the maximum or minimum value of the modulating waves, resulting in all zero states becoming *ST* states (see Figure 2.15 for illustration) [32]. As a result, the voltage stress across the devices can

be highly minimized. While this method offers significant benefits by minimizing voltage stress on the devices (by turning all zero states into *ST* states as shown in Figure 2.15, there is a key drawback. The shoot-through duty cycle constantly changes during inverter operation. This variation leads to high current ripple, which necessitates the use of larger passive components. Consequently, the inverter's size, weight, and cost increase.

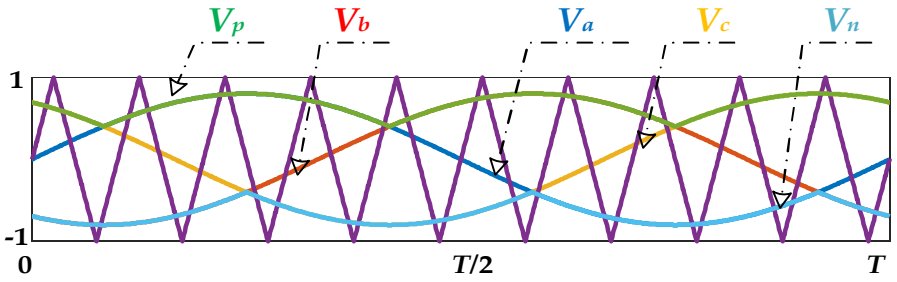


Figure 2.15 MBC method

2.5.1.3 Maximum Constant Boost Control

A method called Maximum Constant Boost Control with third harmonic injection (MCBC), detailed in reference [33] with a circuit diagram in Figure 2.16, offers a clever compromise between two existing methods (SBC and MBC) for controlling a qZSI. The MCBC achieves this by slightly adjusting the *ST* reference levels used in MBC. This adjustment allows MCBC to maintain a consistent *ST* duty cycle during each switching cycle. Compared to SBC, MCBC provides a significant advantage: a higher voltage gains for the qZSI. Even better, MCBC avoids the low-frequency voltage and current ripples that can plague the impedance components in a qZSI when using MBC.

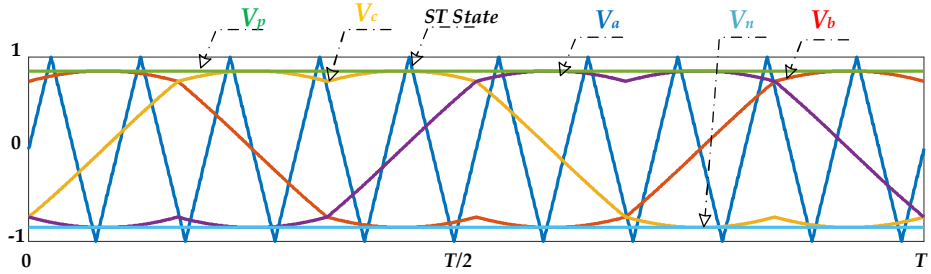


Figure 2.16 Maximum Constant Boost Control with third harmonic injection method

2.5.2 Discontinuous PWM

Discontinuous PWM (DZPWM) actively reduces power losses in ISI. It achieves this by strategically switching only two of the three phases at a time, minimizing the number of switching transitions required by the inverter bridge. This approach has sparked significant research interest, leading to the proposal of numerous new DZPWM techniques [34], [35].

2.5.2.1 Maximum Boost Discontinuous Space Vector Strategy

To boost efficiency in three-phase qZSI, the maximum boost discontinuous space vector strategy (MBDSV) strategy with single-phase leg *ST* was proposed to minimize switching losses and improve power electronics device reliability. This approach strategically utilizes the *ST* state for the switches during specific intervals [36].

The MBDSV modulation technique works by changing conventional sinusoidal signals and using only three reference signals, V_a, V_b, and V_c. These reference signals are compared to a carrier wave to create gate signals for the qZSI switches. The Figure 2.17 illustrates the concept of MBDSV using phase-***a*** as an example.

- S_{ap} is turned on when V_a is higher than the carrier wave, and S_{an} is turned *ON* when V_a is lower than the carrier wave, as shown in Figure 2.18.
- To achieve the *ST* state, S_{an} is kept on when V_a is lower than both the carrier-wave and the V_b and V_c references. as shown in Figure 2.18.

Where, phase *a* is controlled by two switches: S_{ap} (upper) and S_{an} (lower)

The following benefits result from applying the MBDSV modulation strategy:

1) Fewer switch commutations than with traditional modulation techniques (one leg of the qZSI is clamped for one-third of the fundamental time).
2) Single phase-leg *ST*.

However, the following limitations exist:

1) *ST* duty cycle is variable
2) Low-frequency elements are induced in capacitor voltages and inductor currents, which must be reduced by using a high inductance and capacitance.

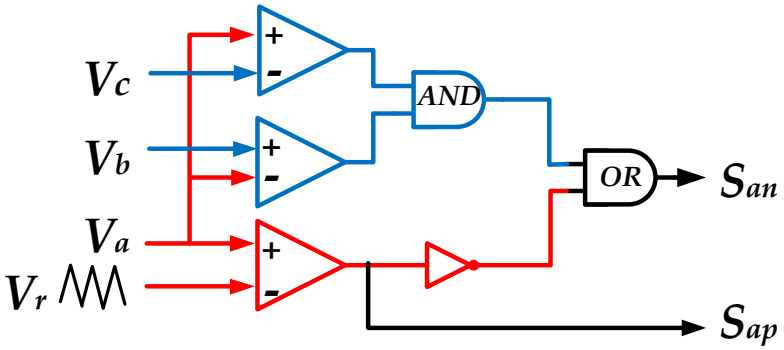


Figure 2.17 Flowchart of the maximum boost discontinuous space vector strategy for phase-***a***.

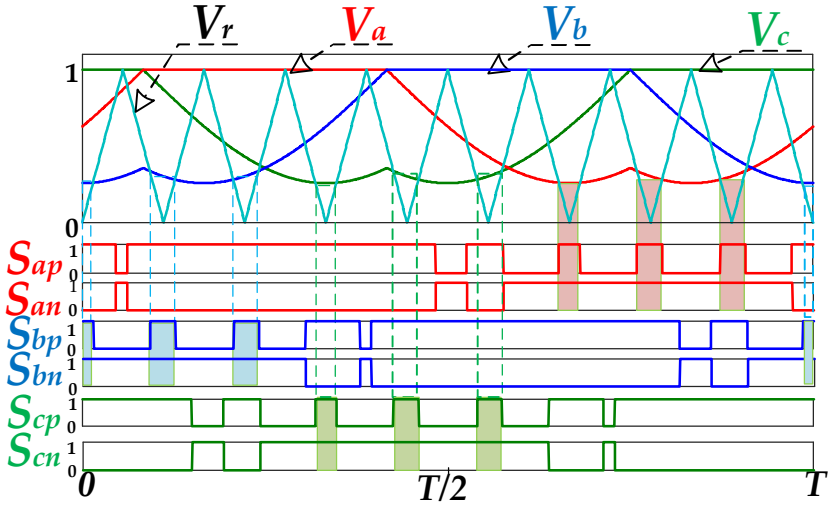


Figure 2.18 Switching signal generation for the maximum boost discontinuous space vector strategy technique ($M = 0.7$, $f_S = 450$ Hz).

2.5.2.2 Discontinuous PWM

Traditional modulation techniques have limitations due to the interconnectedness of the D_{ST} and M. To address this, a new three-phase leg *ST* discontinuous pulse-width modulation (DCPWM) technique for the ZSI has been introduced. The key feature of DCPWM is the separation between the *ST* duty cycle and M. This allows maintaining M at its maximum value, providing greater control flexibility. A new parameter, denoted by K, plays a crucial role in determining both the *ST* duty cycle and the boosting factor [37], [38]. The DCPWM technique relies on three-phase reference signals (V_a, V_b, V_c) as shown in Figure 2.19. These signals are derived in two steps:

1. The first step involves calculating the average of the maximum and minimum values of the sinusoidal reference voltages (V_{ao}, V_{bo}, V_{co}) for each phase.
2. Next, a zero-sequence voltage component (V_{zs}) is incorporated.

Equations (2.27), (2.28), and (2.29) detail the mathematical process for obtaining the reference signals V_a, V_b, and V_c.

The reference sinusoidal voltages V_{ao}, V_{bo}, and V_{co} are given as:

$$\begin{cases} V_{ao} = M.\sin(wt) \\ V_{bo} = M.\sin(wt - 2\pi/3) \\ V_{co} = M.\sin(wt + 2\pi/3) \end{cases} \tag{2.27}$$

The zero-sequence voltage component (V_{zs}) can be calculated as follows:

$$\begin{aligned} V_{zs} = \frac{1}{2}(1 - \operatorname{sgn}(\frac{d}{dt}\max(V_{ao}, V_{bo}.V_{co}))\max(V_{ao}, V_{bo}.V_{co}) + \\ \frac{1}{2}(1 - \operatorname{sgn}(\frac{d}{dt}\min(V_{ao}, V_{bo}.V_{co}))\min(V_{ao}, V_{bo}.V_{co}) \end{aligned} \tag{2.28}$$

Where: "*sgn*" is the sign function, which yields "1" for positive values and "−1" for negative values.

As shown in equations (2.27) and (2.28), the modulating reference signals can be mathematically represented as

$$\begin{cases} V_a = V_{ao} - V_{zs} \\ V_b = V_{bo} - V_{zs} \\ V_c = V_{co} - V_{zs} \end{cases} \tag{2.29}$$

Two envelope signals, V_p and V_n, are essential for generating the *ST* state in the ZSI. These signals are mathematically derived as shown in (2.30).

$$\begin{cases} V_p = \max(V_a, Vb, Vc) + K(1 - ceil(\max(Va, Vb, Vc)) \\ V_n = \min(V_a, Vb, Vc) + K(1 - floor(\min(Va, Vb, Vc)) \end{cases} \tag{2.30}$$

When the DC offset, denoted by K, falls within the range of 0 to 0.5 (as illustrated in Figure 2.20), the '*ceil*' and '*floor*' functions are used to determine the closest integer above and below the real number K, respectively

The DCPWM technique adjusts the DC offset (represented by K) to its maximum value (M) in order to achieve the desired voltage boost. Typically, the D_{ST} increases as K decreases, and consequently, the boosting effect is amplified. In this specific case, M is set to its highest possible value (M_{max}). To generate the envelope signals V_p and V_n, the zero periods within the signals for the maximum (V_a, V_b, V_c) and minimum (V_a, V_b, V_c) of the three phases (V_a, V_b, V_c) are modified by adding K and subtracting K, respectively.

Figures 2.19 and 2.20 illustrate the flowchart of the DCPWM technique for each phase (*a*, *b*, and *c*). The core principle of modulation works as follows:

- Switches S_{ap}, S_{bp}, and S_{cp} are turned *ON* when the voltage phase (V_a, V_b, or V_c) is higher than the carrier wave V_r (refer to Figures 2.19 and 2.20). Conversely, switches S_{an}, S_{bn}, and S_{cn} are activated when the corresponding phase voltage is lower than the carrier wave.
- To achieve the desired switching times (*ST* states), switches S_{ap}, S_{bp}, and S_{cp} are turned on when the envelope signal V_p falls below the carrier signal V_r. In contrast, switches S_{an}, S_{bn}, and S_{cn} are activated when the envelope signal V_n rises above the carrier wave, as depicted in Figures 2.19 and 2.20.

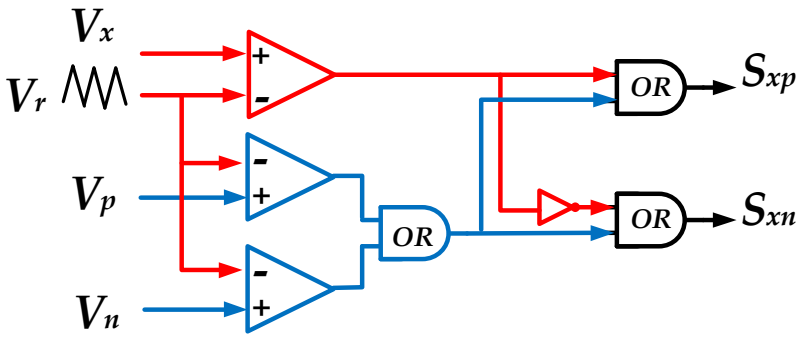


Figure 2.19: Flowchart of the discontinuous pulse-width modulation for phase-*x* (where *x*=*a*, *b* or *c*)

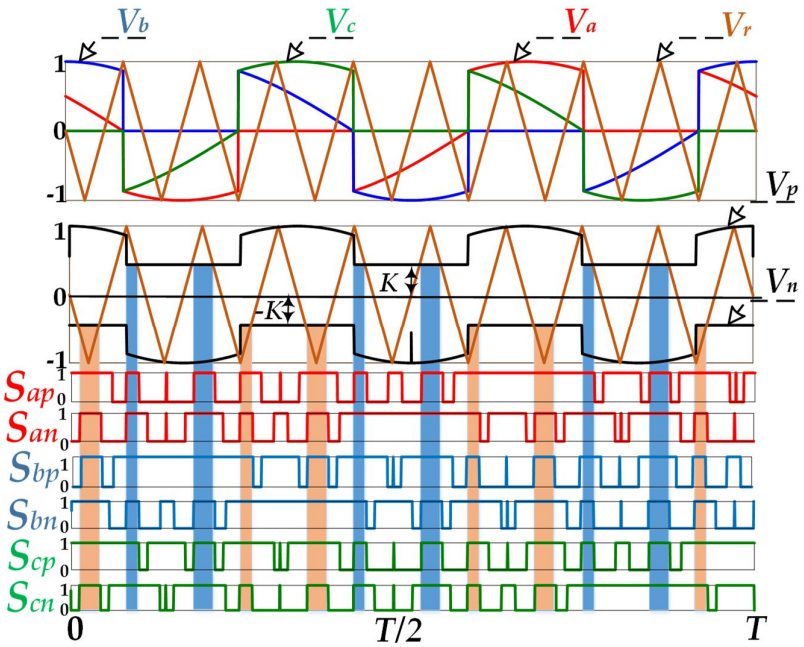


Figure 2.20: Switching signal generation for the discontinuous pulse-width modulation technique ($M = 1/\sqrt{3}$, f_S= 450Hz, K=0.4)

The DCPWM technique offers several advantages:

1. Independent control of *ST* duty cycle and boosting factor: This allows *M* to be fixed at its highest setting, providing more control over the output voltage.
2. High voltage gain without compromising output current quality: DCPWM achieves high voltage gains without requiring a reduction in the *M*.

3. Reduced current ripple and improved DC-link efficiency: DCPWM eliminates the low-frequency component in the inductor current, leading to smoother current flow (reduced ripple).
4. Lower switching losses: By keeping the switches locked in the on state for one-third of the fundamental period (π/3).

On the other hand, the following demerits exist:

1. Increased control complexity: DCPWM requires two additional control signals to generate the desired switching times (*ST* states).
2. Potential for voltage stress and distortion: Low maximum modulation index value (M=$1/\sqrt{3}$) leads to high voltage stress and deteriorates the THD.

2.5.2.3 Discontinuous Space Vector Modulation

Traditional SVM theory is adapted for ISI to improve low harmonic content and DC-link voltage use [39]. To achieve this in three-phase ISI, a single-phase *ST* leg discontinuous space vector modulation (DZSVM2) method is used. This method reduces switching losses by using fewer switching sequences, achieved by eliminating one zero state [40]. In other words, during switching, one inverter leg is locked to either positive or negative DC voltage, while the others switch. Moreover, *ST* periods are divided equally and spread across the switching cycle, using one inverter leg per interval. This reduces overall switching compared to traditional methods. This is crucial in high-power systems where even small switching loss savings translate to significant energy savings, improving overall drive system reliability and efficiency [41].

Compared to traditional SVM for the three-phase ZSI with six active (V_1 to V_6), and two zero vectors (V_0, V_7), and one *ST* vector (V_{ST}). DZSVM2 uses eight sectors by splitting two sectors into 30° sub-sectors. This allows for higher modulation index control, resulting in lower output current distortion (THD), (See Figure 2.20 for voltage space vectors). Within each sector/sub-sector, switching times for two adjacent vectors determine the reference voltage (V_{ref}) along with the *ST* vector. The mathematical formula for this is

$$V_{ref} = \frac{T_1}{T_{sw}} V_i + \frac{T_1}{T_{sw}} V_{i+1} + \frac{T_0 - T_{ST}}{T_{sw}} V_0 + \frac{T_{ST}}{T_{sw}} V_{ST} \tag{2.31}$$

where T_s is the switching period, T_1 and T_2 are the application times of the adjacent active vectors V_i and V_{i+1}, respectively. T_0 is the time of the zero vector, which contains the conventional zero vector V_0 and V_{ST}. In all sectors, the application times are defined as:

$$\begin{cases} T_1 = M.T_{sw}.\sin(\pi/3 - \theta + (i-1)\pi/3) \\ T_2 = M.T_{sw}.\sin(\theta + (i-1)\pi/3) \\ T_0 = T_{sw} - T_1 - T_2 \end{cases} \tag{2.32}$$

Where 'i' indicates the sector ranges from 1 to 6, the two sub-sector in the second and fifth sector (i = 2 and 5), respectively. θ is the inclined angle of the reference vector voltage V_{ref}, where the modulation index defined as $(M=\sqrt{3}V_{ref}/V_{DC})$.

The DZSVM2 method cuts down on switching losses by using just one zero voltage state (either V_0 or V_7) per sector, along with a clever way to spread out the *ST* state. This reduces the number of switching transitions needed in each sector by one. The DZSVM2 strategy involves placing four *ST* states within each switching cycle, lasting for a quarter of the cycle time (T_{ST}/4), while keeping the active voltage states the same (as shown in Figure 2.21).

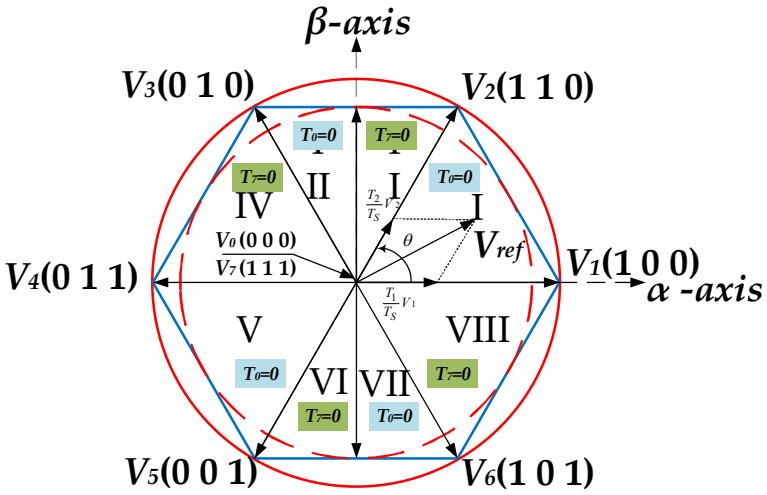
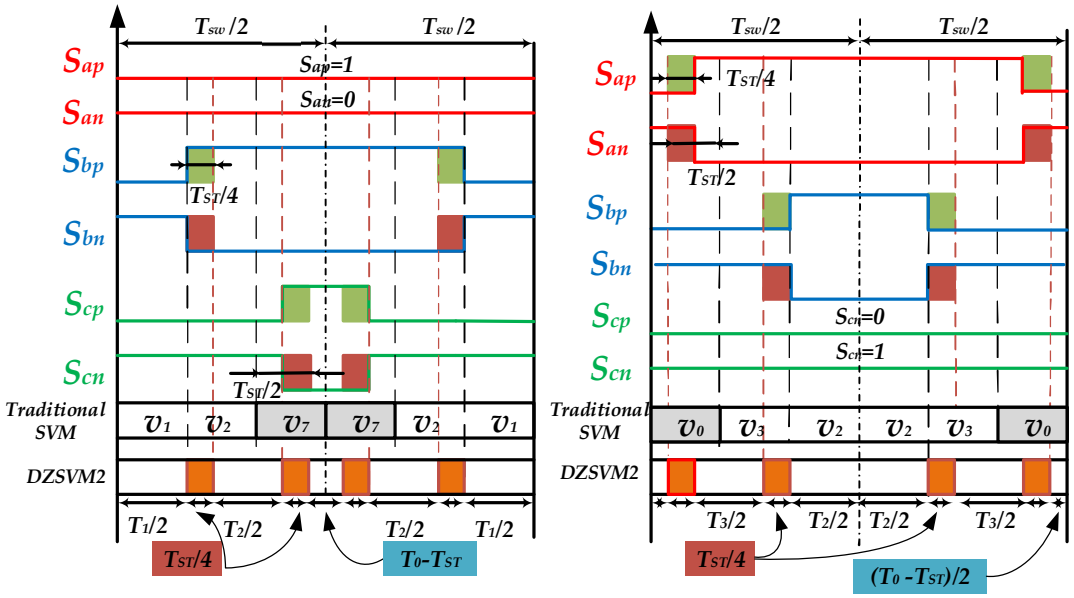


Figure 2.21: Voltage space vector for discontinuous space vector modulation

Figure 2.2(a) and (b) depict switching patterns for sectors 1 (0°–60°) and 2 (60°–90°). In each sector, the DZSVM2 technique keeps one switch of a leg permanently *ON* (e.g., S_{ap} in sector 1) and the other permanently *OFF* (S_{an} in sector 1). By limiting switching in this way, DZSVM2 significantly reduces switching power losses.



(a) (b)

Figure 2.22: Switching sequence for the discontinuous space vector modulation technique for, (a) the first sector (0< θ <60°), (b) the second sector (60°< θ <90°).

The DZSVM2 offers several advantages:

1. It lowers the high-frequency component in the current flowing through the inductors and the voltage across the capacitors.
2. It only requires a single switching operation during the *ST* state.
3. By eliminating one voltage state in each sector, DZSVM2 reduces the overall number of switch transitions.

2. 6 Evaluation of the Modulations Techniques

Table 2. 4 summarizes the different modulation schemes by showing an equivalent figure for each modulation scheme (3P-*ST*, 1P-*ST*). It also presents the average *ST* duty cycle and the boosting factor (B_{max}) in order to calculate the maximum voltage gain (G_{max}) for each scheme. Additionally, the table calculates the normalized peak DC-link voltage (V_{dc}/V_{in}) and compares the current stresses under different strategies.

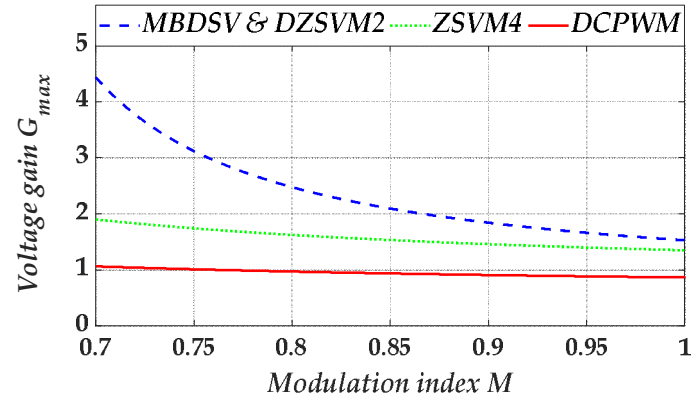
Table 2.4 Comparison Among of the Modulation Strategies

Strategy	SBC	MBC	MCBC	ZSVM4 [39]	MBDSV	DZSVM2	DCPWM
Modulation	Continuous				Discontinuous		
ST Type	3P- *ST* state			1P- *ST* state			3P- *ST* state
N.of reference	3	3	3	6	3	6	5
N.of ST pulses	2	2	2	6	1	4	2
N. of commutations	14	14	14	12	6	8	20
ST duty ratio variation	Constant	Variable	Constant	Constant	Variable	Constant	Variable
D_{ST}	$1-M$	$1-\frac{3\sqrt{3}}{2\pi}M$	$1-\frac{\sqrt{3}}{2}M$	$\frac{3}{4}\left(1-\frac{3\sqrt{3}}{2\pi}M\right)$	$1-\frac{3\sqrt{3}}{2\pi}M$	$1-\frac{3\sqrt{3}}{2\pi}M$	$\frac{3}{4}\left(1-\frac{3\sqrt{3}}{\pi}M\right)$
B	$\frac{1}{2M-1}$	$\frac{\pi}{3\sqrt{3}M-\pi}$	$\frac{1}{\sqrt{3}M-1}$	$\frac{4\pi}{9\sqrt{3}M-2\pi}$	$\frac{\pi}{3\sqrt{3}M-\pi}$	$\frac{\pi}{3\sqrt{3}M-\pi}$	$\frac{2\pi}{6\sqrt{3}M-\pi}$
$G_{max}=B.M$	$\frac{M}{2M-1}$	$\frac{\pi M}{3\sqrt{3}M-\pi}$	$\frac{M}{\sqrt{3}M-1}$	$\frac{4\pi M}{9\sqrt{3}M-2\pi}$	$\frac{\pi M}{3\sqrt{3}M-\pi}$	$\frac{\pi M}{3\sqrt{3}M-\pi}$	$\frac{2\pi M}{6\sqrt{3}M-\pi}$
Voltage stress V_{dc}/V_{in}	$2G_{\max}-1$	$\frac{3\sqrt{3}}{\pi}G_{\max}-1$	$\sqrt{3}G_{\max}-1$	$\frac{9\sqrt{3}G_{\max}-2}{2\pi}$	$\frac{3\sqrt{3}G_{\max}}{\pi}-1$	$\frac{3\sqrt{3}G_{\max}}{\pi}-1$	$\frac{\pi G_{\max}}{6\sqrt{3}G_{\max}-2\pi}$

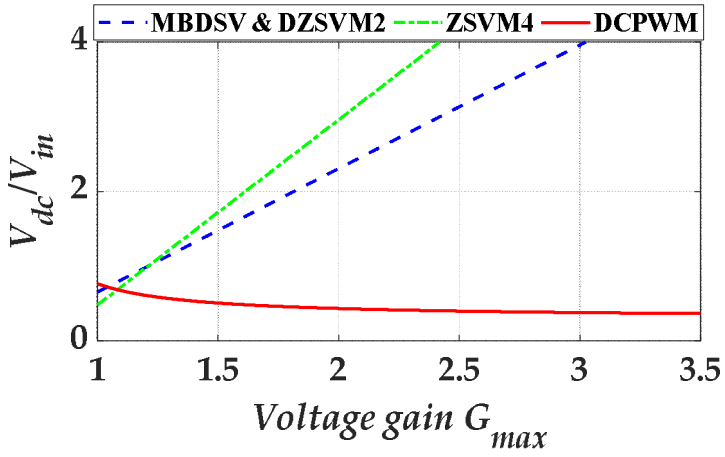
Figure 2.23(a) and (b) depict the relationship between the *M* and the maximum voltage gain (G_{max}), as well as the normalized voltage stress ratio (V_{dc}/V_{in}) and the voltage gain for the CZPWM and DZPWM techniques.

In comparison to the 1P-*ST* CZPWM (ZSVM4) technique, the MBDSV control strategy achieves a superior performance at identical modulation indexes. This is attributed to the MBDSV control's ability to maximize the utilization of traditional zero states. Consequently, the MBDSV control offers a dual benefit: the highest achievable modulation index and the lowest voltage stress across the inverter bridge, for a given voltage gain (as illustrated in Figure 2.23(a) and Table 2.4).

The DCPWM technique employs a fixed value of $K = 0.5$. As shown in Figure 2.23(a), this results in a constant and minimal maximum voltage gain for DCPWM. Furthermore, for a given DC input voltage, DCPWM achieves lower voltage stress on the switches while maintaining the same voltage gain compared to other methods (Figure 2.23(b)). In contrast, ZSVM4, which utilizes a uniformly distributed stationary *ST* state, offers the advantage of eliminating low-frequency ripples associated with the output frequency. However, it comes at the cost of exhibiting the highest voltage stress across the inverter bridge for a given voltage gain.



(a)



(b)

Figure 2.23: Comparison between the presented CZPWM, DZPWM techniques for the qZSI, (a) voltage gain versus the modulation index, (b) voltage stress ratio versus the inverter bridge against the voltage gain.

2.7 Results and Discussions

2.7.1 Steady state Results

To validate the theoretical analysis and assess the performance of CZPWM and DZPWM strategies, simulations were conducted using MATLAB/Simulink. The qZSI output connected to a three-phase inductive load through an *LC* filter (system parameters in Table A.1) was modulated with varying *M* and V_{in} values to achieve a consistent 170V *RMS* phase voltage output. Figure 2.24, 2.25 presents the simulation results for DC-link voltage (V_{dc}), inductor current (i_{L1}), three-phase output current (i_{abc}), and output current THD under each modulation strategy. Peak switch current and low-frequency inductive current ripple (Δi_{L1}) for each strategy are summarized in Table 2.6. As evident from Figure 2.24, 2.25 and Table 2.6, significant variations exist in the inductive currents through L_1. DZSVM2 exhibits the lowest inductor current ripple (Δi_{L1} = 8A) due to its equally distributed stationary states. Conversely, DCPWM suffers from the largest and lowest-frequency current ripple (Δi_{L1} = 17.5A) as confirmed in Figure 2.24.

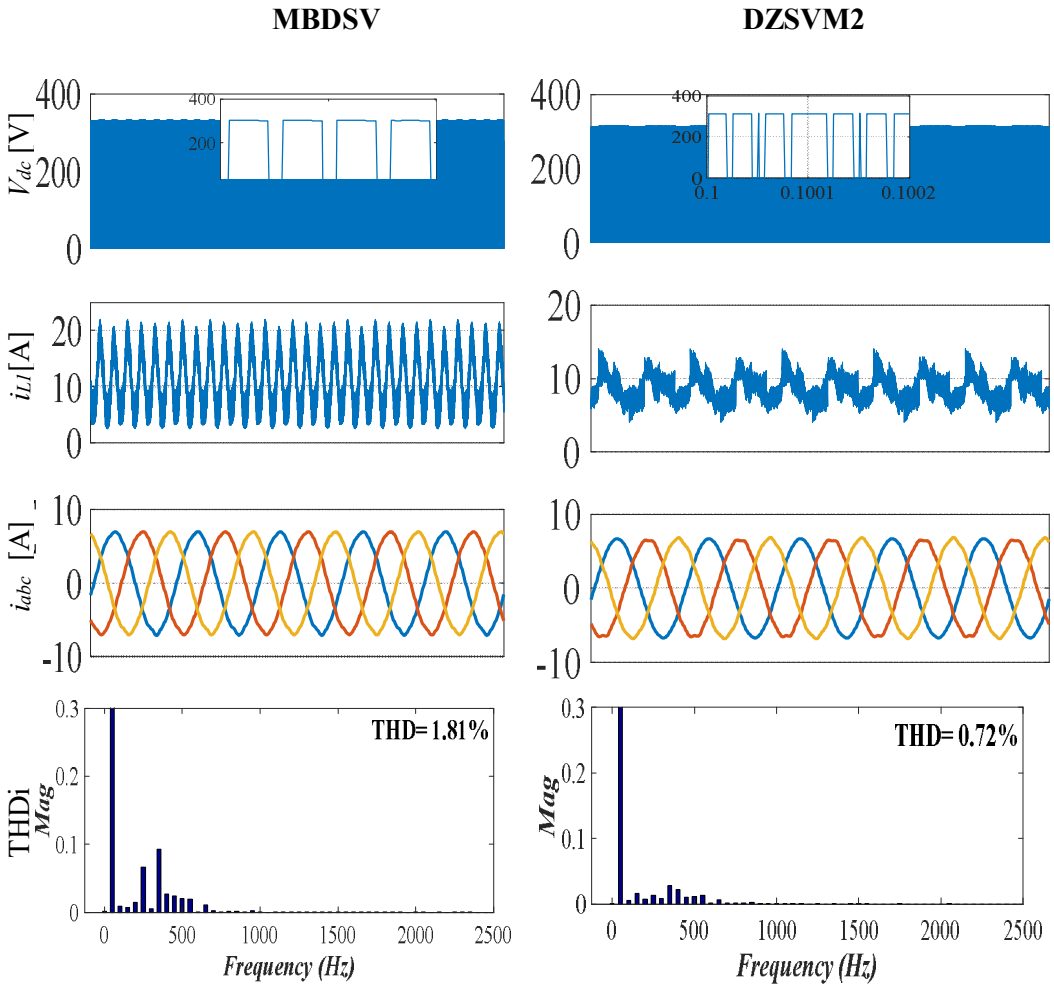
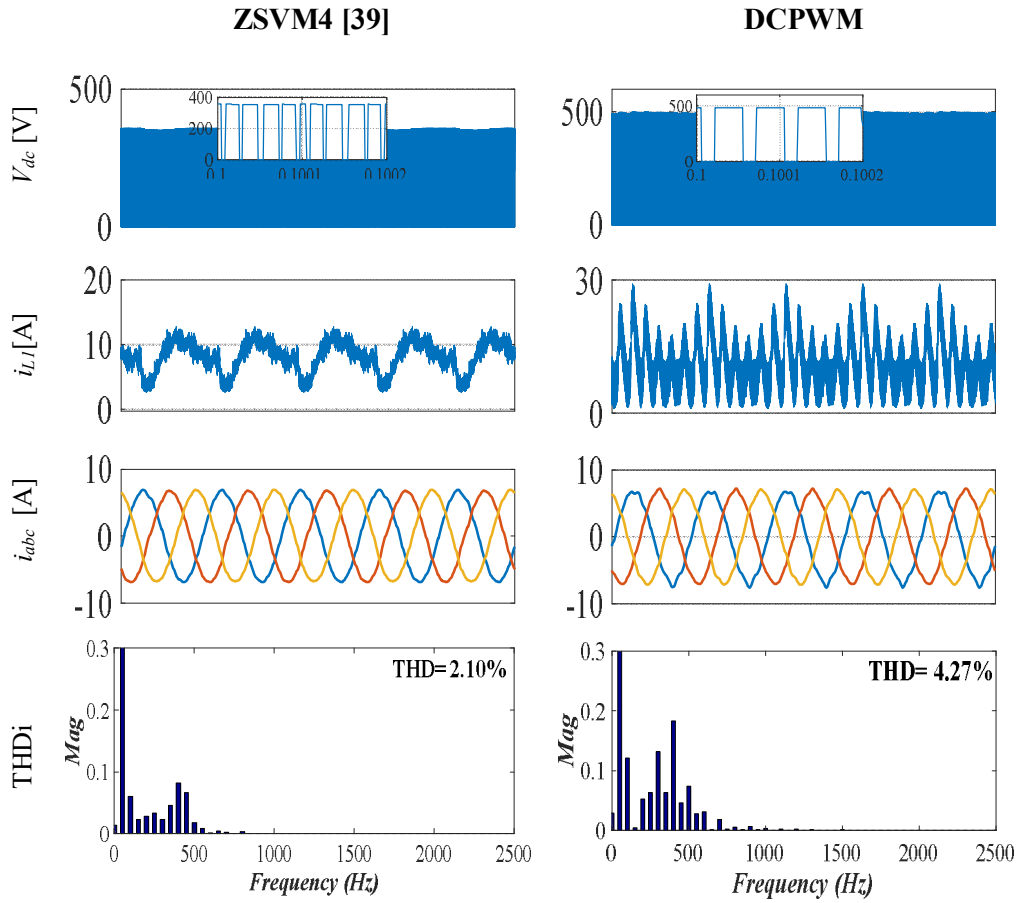


Figure 2.24: Simulation results of three-phase qZSI using MBDSV, DZSVM2 strategies.

An analysis of Table 2.5 reveals that MBDSV, DZSVM2, and ZSVM4 exhibit higher peak switch currents due to their reliance on 1P-*ST* state. Conversely, DCPWM achieves the lowest peak current (18.84 A) by employing a 3P-*ST* state. However, to achieve the same output voltage with a 3P-*ST*, DCPWM necessitates a higher DC-link voltage compared to the other strategies (refer to Figure 2.24, 2.25). This higher DC-link voltage translates to increased voltage stress on the switches according to the used D_{ST} selection technique. It is evident in Figure 2.24, 2.25 that MBDSV, DZSVM2, and ZSVM4 achieve lower THD values in the output currents compared to DCPWM, which can be attributed to their avoidance of a high DC-link voltage.



(b)

Figure 2.25: Simulation results of three-phase qZSI using ZSVM4, and DCPWM modulation strategies.

Table 2.5 Summary of simulated results in different strategies

Modulation	MBDSV		DZSVM2	ZSVM4 [39]	DCPWM
Peak *ST* current [A]	S_{ap} 34.07	S_{an} 40.36	26.03	26.29	18.84
Low frequency Inductive current ripple Δ i_L	15		8	9.5	17.5
THD output current %	1.81		0.72	2.1	4.27

2. 7.2 Power loss calculation

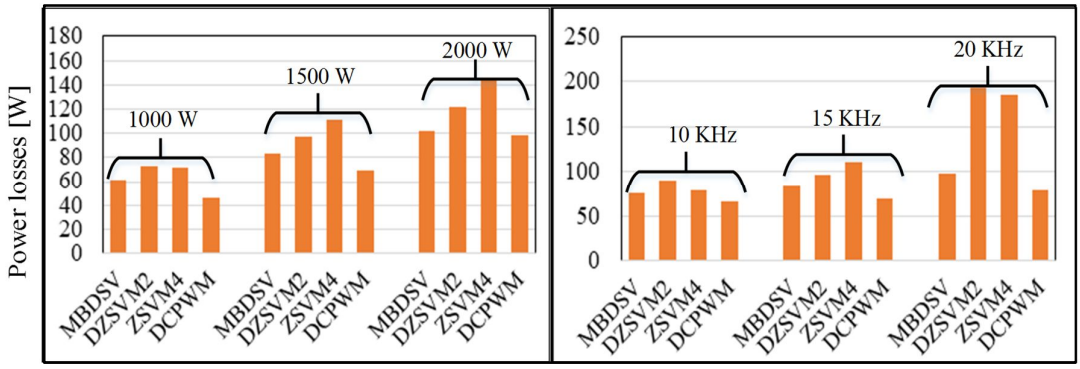
To assess the impact of each modulation strategy on the overall efficiency of the qZSI, the power losses within the converter switches were measured using PLECS. The results are presented in Figure 2.26. The total power loss (P_{Total}) in each modulation technique, as described by

$$P_{Total} = P_{SW\text{-}IGBT} + P_{C\text{-}IGBT} + P_{Total\text{-}D} + P_{Total\text{-}inD} \quad (2.33)$$

where the $P_{SW\text{-}IGBT}$, $P_{C\text{-}IGBT}$, $P_{Total\text{-}D}$, and $P_{Total\text{-}inD}$ are the switching power loss and the conduction power loss in the IGBT, the total loss in the antiparallel diode *D*, and the total loss in the input diode, respectively.

The power loss analysis employed a discrete IGBT model (F4-50R06W1E3 with antiparallel diode). As illustrated in Figure 2.26, DCPWM and MBDSV exhibit the lowest

total power loss across various output power levels compared to the other modulation strategies. Conversely, ZSVM4 consistently incurs the highest power loss. When considering different switching frequencies, ZSVM4 and DZSVM2 experience higher power losses compared to the other techniques. DCPWM remains the most efficient in terms of power loss under these varying conditions.



(a) (b)

Figure 2.26: Power losses of the qZSI using the presented modulation techniques: (a) Versus different output power rates (f_s= 10 kHz), (b) Versus switching frequency (output power is set 1500W).

2.8 Conclusion

This chapter explored various ISI topologies, focusing on existing switched inductors combined with ZSI/qZSI. The analysis compared the advantages and disadvantages of each topology, revealing that SL-ISL-qZSI, SCL-qZSI, and ESL-qZSI achieve the highest boost factor, while ZSI/qZSI achieve the lowest. All these networks are well-suited for single-stage, high-voltage step-up conversion of low DC voltage sources, such as those found in photovoltaic and fuel cell generation systems.

Furthermore, the chapter presented and analyzed carrier-based zero-shoot PWM (CZPWM) and duty-cycle PWM (DZPWM) for the three-phase qZSI. It investigated switching sequences, maximum voltage gains, and switch voltage stress for these methods.

A comparative study evaluated the proposed DZPWM against continuous ZSVM4, considering DC-link utilization, inductive current ripple, current stresses, power losses, and output current THD.

Key findings include:

- MBDSV and DZSVM2 offer higher voltage gain with lower switch voltage stress compared to DCPWM.
- DCPWM exhibits the lowest current stresses due to its 3P-*ST* states compared to the other methods.
- DZSVM2 and ZSVM4 achieve lower inductor current ripples than MBDSV and DCPWM.
- MBDSV, DZSVM2, and ZSVM4 generate lower harmonics compared to DCPWM due to limitations in the modulation index.
- DCPWM experiences lower power losses as switching frequency and output power levels increase.

In conclusion, the chapter provides valuable insights into ZSI topologies and modulation techniques for high-voltage applications. The findings can guide the selection of appropriate ZSI configurations and control strategies for specific requirements.

2.9 Chapter reference

[1] O. Ellabban and H. Abu-Rub, "Z-source inverter: Topology improvements review," *IEEE Ind. Electron. Mag.*, vol. 10, no. 1, pp. 6–24, 2016.

[2] F. Z. Peng, "Z-source inverter," *IEEE Trans. Ind. Appl.*, vol. 39, no. 2, pp. 504–510, 2003.

[3] "Applications in Photovoltaic Power Systems," in *Impedance Source Power Electronic Converters*, 2016. doi: 10.1002/9781119037088.ch14.

[4] D. Mande, J. P. F. Trovão, M. C. Ta, and T. Van Do, "Dual-source bidirectional quasi-Z-Source inverter development for off-road electric vehicles," *World Electr. Veh. J.*, vol. 13, no. 9, p. 174, 2022.

[5] J. Anderson and F. Z. Peng, "Four quasi-Z-source inverters," in *2008 IEEE Power Electronics Specialists Conference*, IEEE, 2008, pp. 2743–2749.

[6] A. Ayad, S. Hanafiah, and R. Kennel, "A comparison of quasi-Z-source inverter and traditional two-stage inverter for photovoltaic application," in *Proceedings of PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, VDE, 2015, pp. 1–8.

[7] A. Abdelhakim, P. Davari, F. Blaabjerg, and P. Mattavelli, "Analysis and Design of the Quasi-Z-Source Inverter for Wide Range of Operation," *2018 IEEE 19th Work. Control Model. Power Electron. COMPEL 2018*, no. June, 2018, doi: 10.1109/COMPEL.2018.8458486.

[8] Y. Li, S. Jiang, J. G. Cintron-Rivera, and F. Z. Peng, "Modeling and control of quasi-Z-source inverter for distributed generation applications," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1532–1541, 2012.

[9] M. Zhu, K. Yu, and F. L. Luo, "Switched inductor Z-source inverter," *IEEE Trans. Power Electron.*, vol. 25, no. 8, pp. 2150–2158, 2010.

[10] M. A. Ismeil, A. Francees, and R. Kennel, "Controller design for improved switched inductor (SL) Z-source inverter for photovoltiac applications," *Int. J. Adv. Renew. Energy Res*, vol. 1, no. 6, pp. 345–353, 2012.

[11] M.-K. Nguyen, Y.-C. Lim, and G.-B. Cho, "Switched-inductor quasi-Z-source inverter," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3183–3191, 2011.

[12] A. Bakeer, M. A. Ismeil, M. Orabi, and R. Kennel, "Control of switched-inductor quasi Z-Source Inverter (SL-qZSI) based on model predictive control technique (MPC)," in *2015 IEEE international conference on industrial technology (ICIT)*, IEEE, 2015, pp. 2248–2253.

[13] L. Li and Y. Tang, "A high set-up quasi-Z-source inverter based on voltage-lifting unit," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, IEEE, 2014, pp. 1880–1886.

[14] V. Jagan and U. Prashanth, "Voltage-Lift-Type Z-Source Inverter," in *International Conference on Electrical and Electronics Engineering*, Springer, 2022, pp. 397–410.

[15] A. Ahmad, R. K. Singh, and V. N. Lal, "A family of enhanced voltage gain switched-boost impedance-source inverter topologies for renewable energy resources," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, IEEE, 2019, pp. 4353–4358.

[16] Y. P. Siwakoti, F. Blaabjerg, and P. C. Loh, "New magnetically coupled impedance (Z-) source networks," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7419–7435, 2015.

[17] H. F. Ahmed, H. Cha, S.-H. Kim, and H.-G. Kim, "Switched-coupled-inductor quasi-Z-source inverter," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1241–1254, 2015.

[18] S. Sharifi and M. Monfared, "Series and tapped switched-coupled-inductors impedance networks," *IEEE Trans. Ind. Electron.*, vol. 65, no. 12, pp. 9498–9508, 2018.

[19] M.-K. Nguyen, Y.-C. Lim, and J.-H. Choi, "Two switched-inductor quasi-Z-source inverters," *IET Power Electron.*, vol. 5, no. 7, pp. 1017–1025, 2012.

[20] M. Ghodsi, S. M. Barakati, and B. Wu, "Extended switched-inductor quasi-Z-source inverter: Modeling and prototype realization," *Int. Trans. Electr. Energy Syst.*, vol. 29, no. 3, p. e2744, 2019.

[21] Y. Wang, Q. Bian, X. Hu, Y. Guan, and D. Xu, "A high-performance impedance-source converter with switched inductor," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3384–3396, 2018.

[22] K. Deng, F. Mei, J. Mei, J. Zheng, and G. Fu, "An extended switched-inductor quasi-Z-source inverter," *J. Electr. Eng. Technol.*, vol. 9, no. 2, pp. 541–549, 2014.

[23] N. Subhani, R. Kannan, A. Mahmud, and F. Blaabjerg, "Z-source inverter topologies with switched

Z-impedance networks: A review," *IET Power Electron.*, vol. 14, no. 4, pp. 727–750, 2021.

[24] N. Priyadarshi, S. Padmanaban, D. M. Ionel, L. Mihet-Popa, and F. Azam, "Hybrid PV-Wind, micro-grid development using quasi-Z-source inverter modeling and control-experimental investigation," *Energies*, vol. 11, no. 9, Sep. 2018, doi: 10.3390/en11092277.

[25] D. Sun, B. Ge, D. Bi, and F. Z. Peng, "Analysis and control of quasi-Z source inverter with battery for grid-connected PV system," *Int. J. Electr. Power Energy Syst.*, vol. 46, pp. 234–240, 2013.

[26] F. Guo, L. Fu, C.-H. Lin, C. Li, W. Choi, and J. Wang, "Development of an 85-kW bidirectional quasi-Z-source inverter with DC-link feed-forward compensation for electric vehicle applications," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5477–5488, 2013.

[27] K. Chitra, K. Viji, and M. Lakshmanan, "Implementation of Solar Photovoltaic System with Switched Inductor Z-Source Inverter," in *International Conference on Signal & Data Processing*, Springer, 2022, pp. 565–580.

[28] R. Seyezhai, K. Arthi, J. Bhavani, A. Archana, and M. Deepa, "Design and control of switched-inductor quasi-Z-source inverter for photovoltaic applications," *Int. Ref. J. Eng. Sci.*, vol. 3, no. 10, pp. 15–28, 2014.

[29] S. S. Kumar and S. Chinnaiya, "Switched Inductor Quasi-z-source Inverter for PMSG based Wind Energy Conversion System," *Int. J. Emerg. Trends Electr. Electron. (IJETEE–ISSN 2320-9569)*, vol. 3, no. 1, pp. 41–46, 2013.

[30] V. Jagan and S. Das, "High boosting type Z-source inverter/improved Z-source inverter for solar photovoltaic system," in *2015 Annual IEEE India Conference (INDICON)*, IEEE, 2015, pp. 1–6.

[31] A. Abdelhakim, F. Blaabjerg, and P: Mattavelli, "Modulation schemes of the three-phase impedance source inverters—Part I: Classification and review," *IEEE Trans. Ind. Electron.*, vol. 65, no. 8, pp. 6309–6320, 2018.

[32] Y. Zhang, X. Ma, J. Liu, Z. Dong, and J. Han, "An Improved Control Strategy for Z-source Inverter with Maximum Boost Capability and Minimum Switching Frequency," pp. 1317–1326, 2015.

[33] M. Shen, J. Wang, A. Joseph, F. Z. Peng, L. M. Tolbert, and D. J. Adams, "Maximum Constant Boost Control of the Z-Source Inverter," pp. 142–147, 2004.

[34] A. Abid, L. Zellouma, M. Bouzidi, A. Lashab, M. T. Boussabeur, and B. Rabhi, "A Comparative Study of Recent Discontinuous Modulation Techniques for Three-Phase Impedance Source Inverter," *SEPOC 2021*, 2021.

[35] P. Liu, J. Xu, M. Sun, J. Yuan, and F. Blaabjerg, "New discontinuous space vector modulation strategies for impedance- source inverter with super ! i or thermal and harmonic performance," *IEEE Trans. Ind. Electron.*, vol. 69, no. 12, pp. 13079–13 089, 2022.

[36] A. Abdelhakim, F. Blaabjerg, and P. Mattavelli, "An improved discontinuous space vector modulation scheme for the three-phase impedance source inverters," *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, vol. 2018-March, no. March, pp. 3307–3313, 2018, doi: 10.1109/APEC.2018.8341577.

[37] M. S. Diab, A. A. Elserougi, A. M. Massoud, A. S. Abdel-Khalik, and S. Ahmed, "A pulsewidth modulation technique for high-voltage gain operation of three-phase Z-source inverters," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 4, no. 2, pp. 521–533, 2015.

[38] A. A. Hossameldin, A. K. Abdelsalam, A. A. Ibrahim, and B. W. Williams, "Enhanced performance modified discontinuous PWM technique for three-phase Z-source inverter," *Energies*, vol. 13, no. 3, 2020, doi: 10.3390/en13030578.

[39] Y. Liu, B. Ge, H. Abu-Rub, and F. Z. Peng, "Overview of space vector modulations for three-phase Z-source/quasi-Z-source inverters," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 2098–2108, 2013.

[40] B. Barathy, A. Kavitha, and T. Viswanathan, "Effective space vector modulation switching sequence for three phase Z source inverters," *IET Power Electron.*, vol. 7, no. 11, pp. 2695–2703, 2014, doi: 10.1049/iet-pel.2013.0903.

[41] I. Chaib, E. M. Berkouk, J.-P. Gaubert, M. Kermadi, N. Sabeur, and S. Mekhilef, "An Improved Discontinuous Space Vector Modulation for Z-source Inverter with Reduced Power Losses," *IEEE J. Emerg. Sel. Top. Power Electron.*, 2020.

Chapter 3

Optimized Modulation Scheme for Four-Leg quasi Z-Source Inverter

This chapter proposes a novel three-dimensional space vector modulation technique specifically designed for a four-leg quasi-Z-source inverter (4L-qZSI). This method, called 3DZSVM, it has three variations (3DZSVM2, 3DZSVM4, and 3DZSVM8) aimed at improving the overall performance of the 4L-qZSI, particularly regarding steady-state operation and reduction of harmonic distortions. By eliminating the need for trigonometric functions and operating within a single sector, this approach optimizes pulse generation and time interval computations

Extensive simulations were conducted to verify the effectiveness of 3DZSVM for the 4L-qZSI. Simulations predict significant advantages of 3DZSVM over conventional CZPWM methods. These include a 50% reduction in both power loss and output voltage distortion (THD). Moreover, 3DZSVM achieves improved output current quality and further reduces power loss (by 40%) and inductive current ripple (by 50%) under unbalanced load conditions. The effectiveness of 3DZSVM is further corroborated by hardware-in-the-loop (HIL) testing using the TMS320F28379D kit, demonstrating its practicality and strong performance, especially under unbalanced loads.

3.1 General introduction

The growing integration of distributed solar and wind power sources in isolated power systems raises concerns about output voltage quality. Meeting technical and performance standards becomes crucial in such scenarios, with regulations like IEEE Standard 1547-2014 mandating a Total Harmonic Distortion (THD) below 5% for current harmonics [1], [2]. Three-phase distribution systems, common in these setups, cater to both three-phase loads (linear or non-linear) and numerous single-phase loads. This mix leads to unbalanced absorbed currents between phases, consequently causing voltage instability.

Unbalanced voltages generate inverse and zero current components, which can negatively impact power quality. The European standard EN 50160 recommends a voltage unbalance factor (VUF) of less than 2% to minimize these adverse effects [3]. Distributed energy generation systems, where power output fluctuates based on demand, are inherently susceptible to unbalanced loading conditions. Such unbalanced loads draw unequal currents from each phase, exceeding the neutral line current capacity in three-phase systems. This phenomenon not only leads to increased harmonic distortion in both system voltage and current [4], [5], but also presents challenges for neutral current management. To address these challenges, various converter topologies can be employed. Three common four-wire VSI configurations are used in such applications: the three-phase three-leg VSI (3L-VSI) with a midpoint capacitor, three-phase H-bridge VSI, and three-phase four-leg VSI (4L-VSI).

The first configuration utilizes a 3L-VSI with split DC-link capacitors [6]. This approach offers an advantage like simplicity and reduced switch count. However, a key limitation of this design is its low DC-link voltage utilization. An uncontrolled ripple voltage at twice the line frequency (2ω) appears on the DC-link, requiring larger capacitors to mitigate current ripple issues [7].

The three-phase H-bridge configuration employs three full-bridge inverters connected to the three-phase four-wire system via single-phase isolation transformers. Unlike the 3L-VSI with split capacitors, this topology allows for a lower DC bus voltage as each H-bridge deals with the single-phase voltage. However, this configuration has drawbacks, including a significant increase in the number of required switching devices and the need for transformers, which adds both complexity and cost [8].

For three-phase-four-wire inverters, the four-leg VSI (4L-VSI) stands out as the most advantageous option due to its superior performance [9], [10]. This topology incorporates an additional leg specifically dedicated to handling the zero-sequence current and voltage components flowing through the neutral wire. The 4L-VSI offers several key benefits: i) enhanced dc-link voltage utilization compared to the 3L-VSI configuration (15% higher), ii) Reduced voltage ripple in the dc-link, iii) Reduced need for a large dc-link capacitor, and iv) compactness in terms of size and volume [11], [12]. The additional leg in the 4L-VSI not only grants superior performance but also expands its control capabilities [5]. Compared to the 3L-VSI that has 8 possible switching states, the 4L-VSI offers 16, providing greater flexibility (2^3 vs. 2^4). These advantages make the 4L-VSI a popular choice in diverse applications, both grid-connected and stand-alone, particularly in distributed generation systems. In grid-tied applications, the 4L-VSI often pairs with an inductive filter, enabling controlled current injection into the grid. Its versatility extends to various grid-connected applications, including shunt active power filters [13] and static var compensator (SVC) with static synchronous compensator (STATCOM) [14]. Similarly, for stand-alone applications like uninterruptible power supplies (UPS) [15] and electric motor drives [16]. The *LC* filter in a 4L-VSI plays a vital role in ensuring well-regulated operation. It effectively smooths out the output

voltage, reducing ripple and improving overall power quality. Additionally, the *LC* filter enhances system stability, making the 4L-VSI less susceptible to disturbances.

While the three-phase qZSI with three legs is useful in various applications [17], it has limitations. A key drawback, which is also a reason for its design, is that it can only handle balanced three-phase loads. In contrast, the 4L-qZSI offers several advantages. These include fault tolerance, improved reliability due to no required dead time, and lower trip current during leg short circuits [18], [19]. Figure 3.1 shows a typical example of how the 4L-qZSI is used in a standalone power system.

Several control schemes have been explored for the 4L-qZSI in the reviewed literature. These schemes often rely on nonlinear controllers, like finite control set-model predictive control (FCS-MPC) [19]–[21]. It offers several advantages: it's easy to understand, handles nonlinearities and constraints, capability to control multiple variables simultaneously, and reacts quickly to transients [22]–[24]. However, its effectiveness depends heavily on an accurate system model. Additionally, FCS-MPC operates at variable switching frequencies due to the absence of a modulation stage. This broad spectrum of frequencies negatively impacts the quality of the power output, introducing unwanted harmonics, which is the main drawback of this approach [25], [26].

Various PWM techniques for the 4L-VSI to improve its performance. One example is Carrier-based PWM (CPWM) [31]. This method creates an unbalanced voltage by injecting an offset voltage (V_{fn}) into the reference voltage for the first three legs. This offset voltage then becomes the reference for the fourth leg [27]. However, this approach has limitations. In contrast, Discontinuous Pulse Width Modulation (DPWM) techniques focus on reducing power losses in the power devices by lowering the switching frequency [28]. Several improvements to DPWM have been proposed to address this. For instance, Selective Harmonics Elimination (SHE) control, described in [29] for a three-phase 4L-VSI, eliminates specific lower-order harmonics in the switching waveform. This approach results in a cleaner output waveform with less THD.

However, SVM offers a more efficient alternative to PWM. SVM provides greater flexibility in optimizing switching waveforms and is easier to implement [30], [31]. For 4L-VSIs, Three-Dimensional Space Vector Modulation (3DSVM) [32] is a common approach. Compared to carrier-based PWM, 3DSVM offers several advantages, including better utilization of the DC power supply (high DC-link exploitation) and lower output distortion [33]. However, despite these advantages, it has certain limitations, including complex modeling and large computation time [27]. Previous research has explored streamlined 3DSVM implementations for 4L-VSIs, aiming to reduce complexity and computational time by utilizing a single voltage space vector prism for determining all switching sequences [34], [35]. However, these approaches have not been applied to the 4L-qZSI. This chapter addresses this gap by introducing a novel 3DZSVM algorithm specifically tailored for the 4L-qZSI.

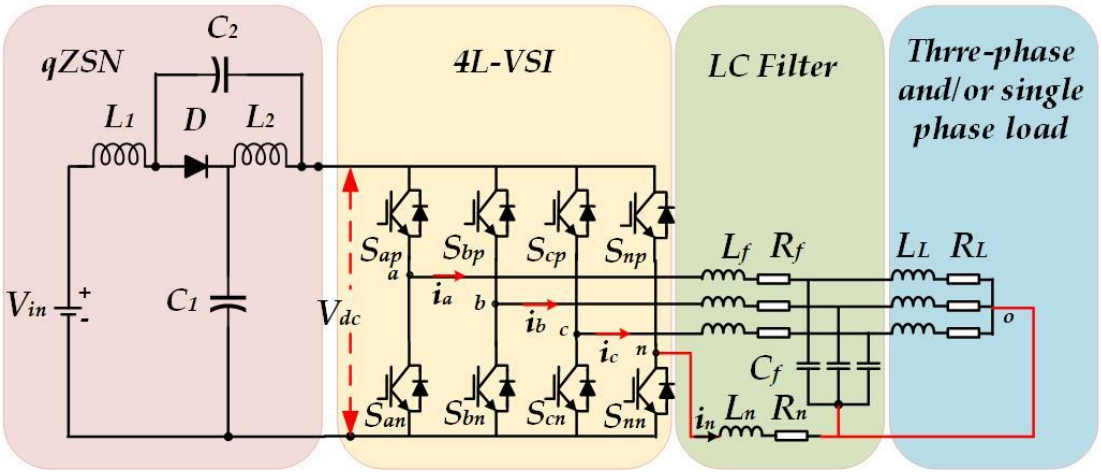


Figure 3.1: 4L-qZSI with an output *LC* filter.

The proposed 3DZSVM technique offers several advantages. It can simultaneously achieve three control objectives: tracking the desired output voltage reference, maintaining the DC voltage at the required level, and compensating for the zero-sequence output current. Furthermore, inspired by the approach used for the four-leg diode clamped converter (4L-DCC) in [36], the 3DZSVM algorithm only needs to be implemented in one sector of the space vector diagram, which simplifies its application. The proposed 3DZSVM algorithm is available in three variants: 3DZSVM8, 3DZSVM4, and 3DZSVM2. These variants depend on the number of inserted *ST*.

This chapter investigates the three 3DZSVM's variants to determine the most effective approach for reducing inductor current ripple in the 4L-qZSI.

Two main contributions are presented in this chapter. The first one is to introducing a new 3DZSVM algorithm specifically designed for the 4L-qZSI, while the second one is exploring three 3DZSVM's variant.

The chapter is organized as follows: Section 3.2 outlines the design and operation of the 4L-qZSI. Section 3.3 introduces the core concept of 3DZSVM. Section 3.4 delves into the details of the proposed 3DZSVM tailored for the 4L-qZSI. Section 3.5 validates the performance of the proposed 3DZSVM through MATLAB/PLECS simulations the 4L-qZSI, comparing power losses to the CZPWM strategy. Section 3.6 further validates the advantages of the 3DZSVM method through Hardware-in-the-Loop (HIL) simulations. Finally, Section 3.7 concludes the chapter with key findings.

3.2 Four Leg-Quasi Z-Source Inverter Topology

As illustrated in Figure 3.1, the 4L-qZSI with an *LC* output filter is analyzed in two stages. In the initial stage, a qZSN, utilizing *LC* components, boosts the DC voltage during switching events. The subsequent stage, a 4L-VSI with an *LC* filter, connects the load's neutral point to the fourth leg's midpoint to facilitate zero-sequence current flow [12]. The 4L-qZSI and load neutrals are denoted by 'n' and 'o', respectively. To streamline the analysis, the following voltage and current vectors are defined

The four control signals, S_a, S_b, Sc, and S_n, generate a total of 16 (2^4) active states for the converter. However, to accommodate the specific requirements of this application, an additional *ST* state is necessary. This results in a total of 17 switching states. Figure 3.2 and Table 3.1, respectively, illustrate the voltage vectors and valid switching states for the 4L-qZSI . The output voltages can be expressed as follows:

$$\begin{cases} V_{an} = (S_a - S_n)V_{dc} \\ V_{bn} = (S_b - S_n)V_{dc} \\ V_{cn} = (S_c - S_n)V_{dc} \end{cases} \tag{3.1}$$

where V_{dc} represents the input DC voltage. The output 4L-qZSI voltages, load voltages, output inverter currents, and load currents can be expressed in vector form as

$$\begin{cases} V_{an} = \begin{bmatrix} V_{an} & V_{bn} & V_{cn} \end{bmatrix}^T \\ V = \begin{bmatrix} V_a & V_b & V_c \end{bmatrix}^T \\ i = \begin{bmatrix} i_{oa} & i_{ob} & i_{oc} \end{bmatrix}^T \\ i_L = \begin{bmatrix} i_a & i_b & i_c \end{bmatrix}^T \end{cases} \tag{3.2}$$

By utilizing Kirchhoff's voltage and current rules to analyze the nodes depicted in Fig. 1, we can derive the load dynamics as follows:

$$V = R_f i + L_f \frac{di}{dt} + V_i - R_n i_n - L_n \frac{di_n}{dt} \tag{3.3}$$

$$i = i_o + C_f \frac{dV}{dt} \tag{3.4}$$

The calculation of the neutral current flowing through the neutral leg is determined by;

$$i_n = -(i_a + i_b + i_c) \tag{3.5}$$

The inductive and capacitive filter concepts may be represented in state-space form by solving equations (3.3), (3.4), and (3.5).

$$\frac{d}{dt}\begin{bmatrix} V \\ i \end{bmatrix} = A\begin{bmatrix} V \\ i \end{bmatrix} + B\begin{bmatrix} V_i \\ i_o \end{bmatrix} \tag{3.6}$$

where

$$A = \begin{bmatrix} 0 & I/C_f \\ -1/L_{eq} & -R_{eq}/L_{eq} \end{bmatrix}, B = \begin{bmatrix} 0 & -I/C_f \\ -1/L_{eq} & 0 \end{bmatrix} \tag{3.7}$$

where

$$R_{eq}=\begin{bmatrix} R_f+R_n & R_f & R_f \\ R_f & R_f+R_n & R_f \\ R_f & R_f & R_f+R_n \end{bmatrix},\ L_{eq}=\begin{bmatrix} L_f+L_n & L_f & L_f \\ L_f & L_f+L_n & L_f \\ L_f & L_f & L_f+L_n \end{bmatrix} \quad (3.8)$$

In this case, I and 0 are third-order unit matrices and zeros, correspondingly. Each switching state corresponds to a certain value of V_i, as indicated in Table 3.1. As a result, the load voltage varies among the 16 switching states in *abc* coordinates.

Table 3.1 4L-qZSI switching states and their associated output voltages in the *abc* coordinates

Switching states					**Voltage vector**		
V_i	S_a	S_b	S_c	S_n	V_{an}	V_{bn}	V_{cn}
V_0	1	0	0	0	V_{dc}	0	0
V_1	0	1	0	0	0	V_{dc}	0
V_2	1	1	0	0	V_{dc}	V_{dc}	0
V_3	0	0	1	0	0	0	V_{dc}
V_4	1	0	1	0	V_{dc}	0	V_{dc}
V_5	0	1	1	0	0	V_{dc}	V_{dc}
V_6	1	1	1	0	V_{dc}	V_{dc}	V_{dc}
V_7	0	0	0	1	- V_{dc}	- V_{dc}	- V_{dc}
V_8	1	0	0	1	0	-V_{dc}	- V_{dc}
V_9	0	1	0	1	- V_{dc}	0	- V_{dc}
V_{10}	1	1	0	1	0	0	-V_{dc}
V_{11}	0	0	1	1	- V_{dc}	- V_{dc}	0
V_{12}	1	0	1	1	0	- V_{dc}	0
V_{13}	0	1	1	1	- V_{dc}	0	0
V_{14}	1	1	1	1	0	0	0
V_{15}	0	0	0	0	0	0	0
V_{ST}	1	1	1	1	0	0	0

3.3 Conventional 3DSVM for the 4L-VSI

Three-dimensional space vector modulation (3DSVM), developed by Richard Zhang [32], [37] is a popular PWM technique for unbalanced loads in three-phase 4L-VSIs. It achieves an average output voltage vector that matches the desired reference voltage vector. This is done by strategically selecting four adjacent switching vectors in the $\alpha\beta\gamma$ space during each switching period. Figure 3.2 depicts these switching vectors for the 4L-VSI. To convert between the three-phase *abc* and $\alpha\beta\gamma$ coordinates, Clarke transformation is employed.

$$\begin{bmatrix} V_\alpha \\ V_\beta \\ V_\gamma \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{3.9}$$

Figure 3.2 illustrates the 4L-VSI's switching vectors in $\alpha\beta\gamma$ space. These 14 vectors form a graphic domain resembling six prisms. Two zero vectors (1111 and 0000) occupy the center layer. The remaining 14 active vectors are distributed across seven layers based on their $V\gamma$ voltage levels. $V\gamma$, representing the zero-sequence component, depends on the neutral current value. Research in [32] compared two switching strategies and found the Class II center-aligned approach to be ideal for real-time applications due to its balance between switching loss and harmonic distortion.

The reference voltage vector (V_{ref}), denoted as $[V_\alpha, V_\beta, V_\gamma]^T$, can have balanced or unbalanced components, and can be either sinusoidal or non-sinusoidal. When the components are balanced and sinusoidal, the trajectory of V_{ref} in the $\alpha\beta$ plane ($V\gamma = 0$) becomes a circle, resembling the conventional SVM circle. Under unbalanced load conditions, however, the trajectory of V_{ref} transforms into an ellipse with an incline, as shown in Figure 3.3.

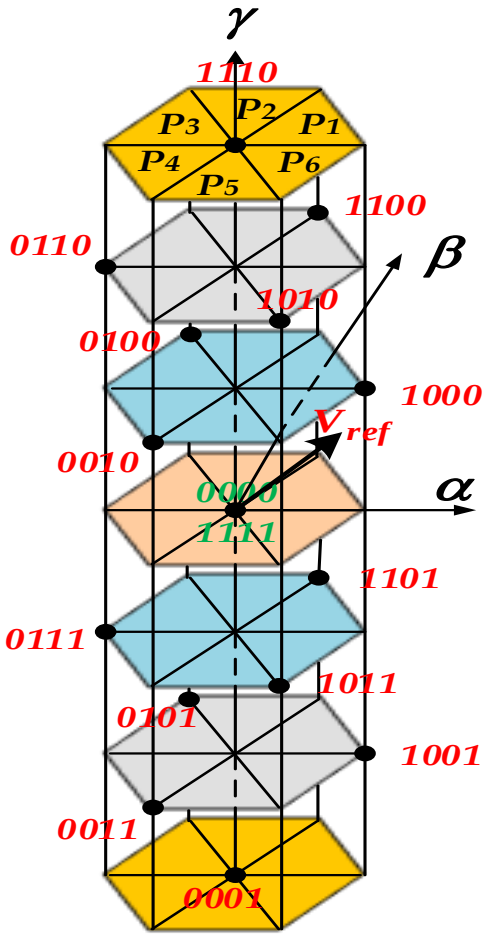


Figure 3.2: Switching vectors of 3DSVM.

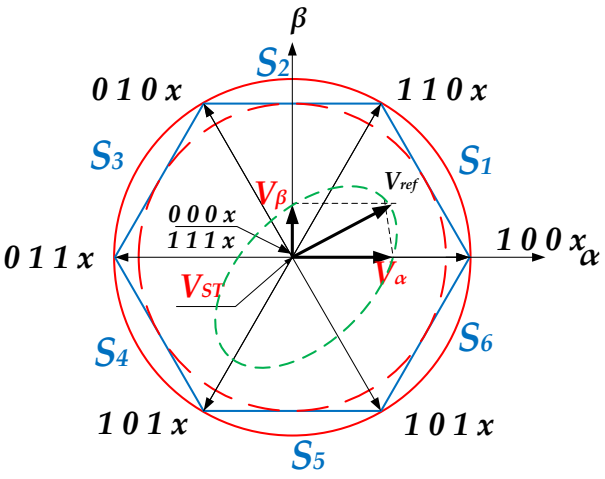


Figure 3.3 Vertical projection on $\alpha\beta$ plan (x can be 0 or 1)

3.4 Proposed optimized 3DZSVM for 4L-qZSI

Similar to ZSVM for the qZSI, three core steps are involved in building the reference voltage vector using SVM algorithms for both 3L-VSIs and 4L-VSIs:

1. Reference vector location
2. Switching times calculation
3. Switching sequence definition

The first two steps are identical between SVM and ZSVM. The key distinction lies in the third step, where SVM defines the switching sequence for the 3L-VSI or 4L-VSI, whereas ZSVM focuses on incorporating the *ST* state into the switching sequence for the qZSI [38]. This section dives deeper into this third step and how the ST state is integrated into the switching sequence for the SVM algorithm.

To streamline computations for the proposed 3DZSVM in the 4L-qZSI, this approach leverages the optimized 3DSVM algorithm from [36]. This method, originally developed for a 4L-DCC, simplifies the traditional 3DSVM by restricting calculations to a single sector of the space vector diagram. As a result, the three steps typically involved in 3DSVM (mentioned earlier) are only performed within this one sector, significantly reducing computational burden. The following subsections will detail these three steps within the context of the proposed 3DZSVM for the 4L-qZSI.

3.4.1 Reference Voltage Vector Location

The V_{ref} needs to be transformed before determining its location. This reconstruction ensures it resides within the first sector (S_1) of the space vector diagram (SVD) to simplify calculations [36]. The original reference voltage vector (ORVV) denoted as $V^*(v_a^*, v_b^*, v_c^*)$ is converted to a reconstructed reference voltage vector (RRVV) denoted as $U^*(U_a^*, U_b^*, U_c^*)$. Table 3.2 and Figure 3.4 illustrate how the RRVV

components are derived based on the sector containing the original vector's components (v_a*, v_b*, v_c*).

Table 3.2 Selecting the components of the RRVV

	S1	S2	S3	S4	S5	S6
U^*_a	v^*_a	v^*_b	v^*_b	v^*_c	v^*_c	v^*_a
U^*_b	v^*_b	v^*_a	v^*_c	v^*_b	v^*_a	v^*_c
U^*_c	v^*_c	v^*_c	v^*_a	v^*_a	v^*_b	v^*_b

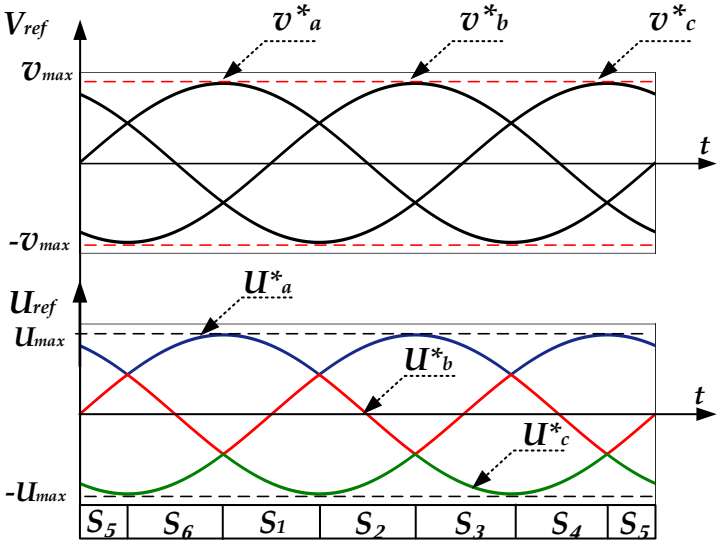


Figure 3.4 Reconstructed reference voltage vector (RRVV)

For the *m*-level 4L-DCC, all tetrahedrons situated in S_1 of the SVD can be categorized into six types [36]. These form two adjoining prisms (PR^1 and PR^2), as depicted in Figure 3.5. These neighboring prisms create a 3D parallelepiped with eight switching vectors (SWVs) v_1, v_2, ..., v_8. Here, TeT^j_i represents the i^{th} tetrahedron situated within the j^{th} prism, PR^j).

In the case of two-level 4L-VSI (m=2), the PR^2 in Figure 3.5(a) does not exist, and therefore, only three types of tetrahedrons remain to be identified ($T_eT^1_1$, $T_eT^1_2$, and $T_eT^1_3$ (see Figure 3.5(b)). Therefore, the axes called ρ-σ-τ (see Figure 3.5(a) [36]) are used to i) identify the type of tetrahedron, ii) select the appropriate SWVs, and iii) calculate the corresponding switching times.

By putting m=2 for two-level 4L-VSI, it yields:

$$\begin{bmatrix} U^*_\rho \\ U^*_\sigma \\ U^*_\tau \end{bmatrix} = \frac{m-1}{V_{dc}} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} U^*_a \\ U^*_b \\ U^*_c \end{bmatrix}, m = 2 \tag{3.10}$$

The fractional parts of the components of the RRVV U^* in (3.10) are denoted by p, q, and r. Based on these values, the tetrahedron type for two-level 4L-VSI is easily identified, as illustrated in Figure 3.6.

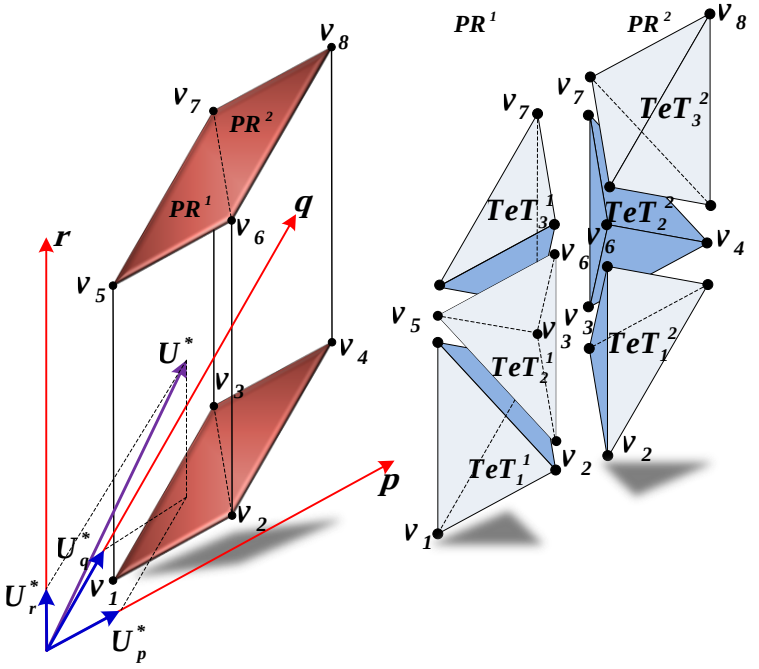


Figure 3.5 (a) Three-dimensional parallelepiped, (b) the six categories of tetrahedrons [36].

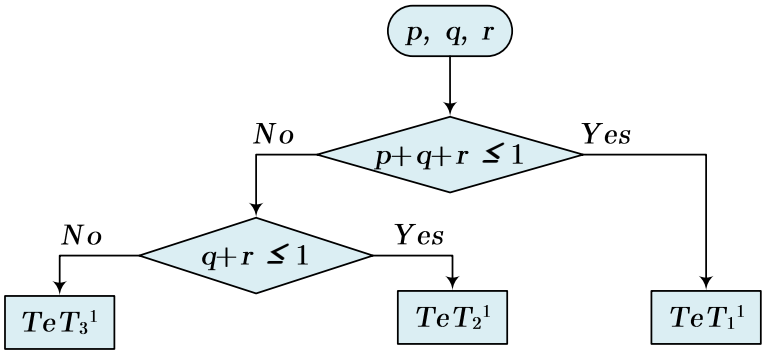


Figure 3.6. Tetrahedron type identification process (Particular case for 2-level 4L-VSI)

3.4.2 Switching times calculation

Within each switching period (T_{sw}), the 3DSVM algorithm selects neighboring switching vectors (SWVs) surrounding the RRVV. Subsequently, the algorithm determines the optimal switching time for each SWV, ensuring that the average output voltage matches its reference value during each switching period.

Based on [36], the switching times are derived using simple expressions corresponding to the different Tetrahedron types, as outlined in Table 3.3.

Table 3.3 Duration periods of the neighboring switching vectors.

	Tetrahedron types		
	TeT¹₁	***TeT¹₂***	***TeT¹₃***
Adjacent vectors	v_1 v_2 v_3 v_5	v_6 v_2 v_3 v_5	v_6 v_7 v_3 v_5
Time intervals	$T_1=T_s(1-p-q-r)$ $Tt_2=T_sp$ $Tt_3=T_sq$ $Tt_5=T_sr$	$T_6=T_s(p+q+r-1)$ $T_2=T_s(1-q-r)$ $T_3=T_sr$ $T_5=T_s(1-q-q)$	$T_6=T_sp$ $T_2=T_s(q+r-1)$ $T_3=T_s(1-r)$ $T_5=T_s(1-p-q)$

3.4.3 Switching Sequence Definition

The 3DZSVM implementation for a 4L-qZSI requires a modification compared to the standard 3DSVM. To account for the *ST* state, a new duration (T_{ST}) needs to be incorporated alongside the existing switching times (T_1, T_2, T_3, and T_0) used in the 3DSVM. This additional duration allows switching between the *ST* state and active states, enabling the charging and discharging of capacitors and inductors in the 4L-qZSI. The 3DZSVM algorithm used in the 4L-qZSI switching process incorporates 14 active voltage vectors, two standard zero vectors, and an additional *ST* vector (V_{ST}). The reference voltage vector for the 4L-qZSI within each tetrahedron is defined as.

$$V_{ref} = V_1T_1 / T_{Sw} + V_2T_2 / T_{Sw} + V_3T_3 / T_{Sw} + V_0T / T_{Sw} + V_{ST}T_{ST} / T_{Sw} \tag{3.11}$$

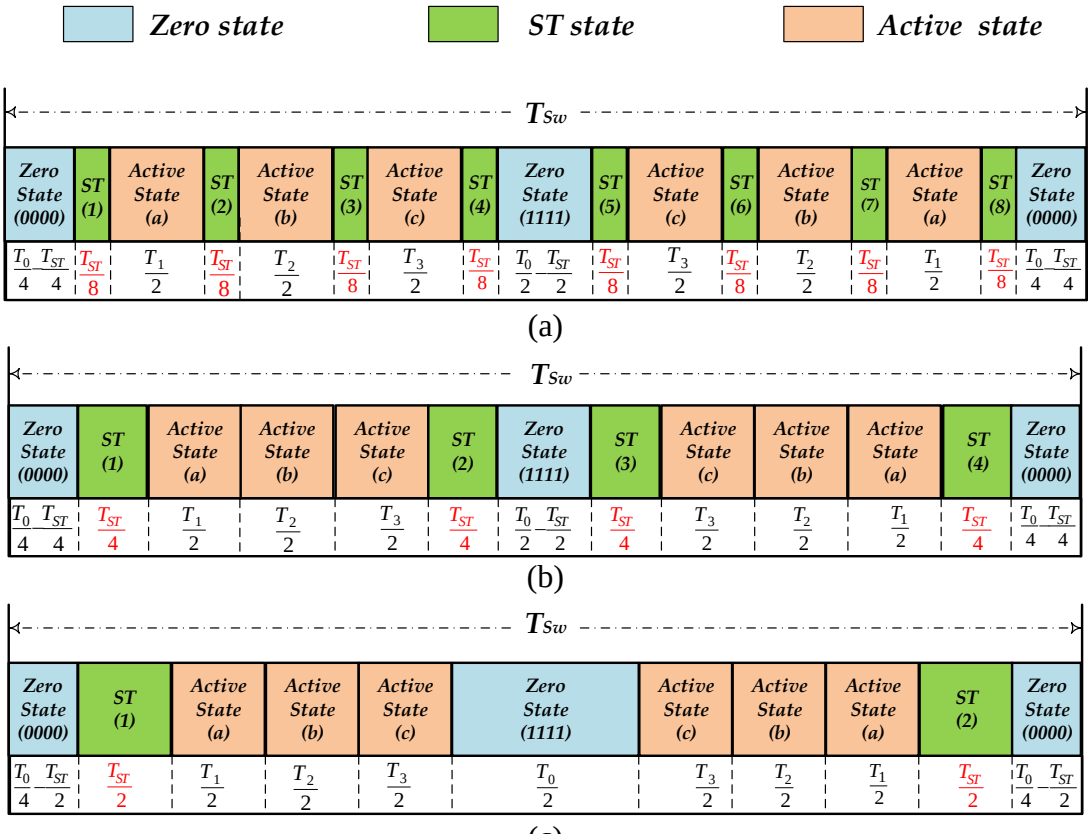


Figure 3.7 Switching pattern for 4L-qZSI for different modulation schemes (a) 3DZSVM8, (b) 3DZSVM4, and (c) 3DZSVM2.

To improve the DC-link voltage in the 4L-qZSI and achieve the desired AC output voltage, the 3DZSVM implementation incorporates a technique to minimize extra switching and related energy losses. This is achieved by strategically placing the *ST* intervals. These ST intervals are inserted either before or after the start/end times of the active switching times (T_1, T_2, T_3). The total desired *ST* duration is then distributed evenly throughout the switching period. This even distribution is accomplished by activating only two switches in a single phase leg at a time during the *ST* state.

The proposed 3DZSVM for the 4L-qZSI offers an alternative strategy called 1P-*ST*. This method introduces *ST* states within a single leg during the zero-state intervals of the standard 3DZSVM. The number and placement of these *ST* periods within a switching cycle can be varied to create different schemes. Three such schemes are introduced: 3DZSVM8, 3DZSVM4, and 3DZSVM2, which incorporate (8, 4, and 2) *ST* periods per switching cycle, respectively. Figure 3.7(a)-(c) illustrates the distinct switching patterns associated with each scheme.

Different switching sequences are employed to achieve a clean output voltage waveform with minimal harmonic distortion. These sequences strategically distribute the on-time for a specific voltage state throughout a control period.

Figures 3.7(a), (b), and (c) illustrate this concept for the 3DZSVM8, 3DZSVM4, and 3DZSVM2 configurations, respectively. Each figure showcases how the total *ST* state time is divided for that specific configuration.

- 3DZSVM8: Achieves eight equal portions within a control period, incorporating each *ST* duration into zero-to-active state transitions. This allows all 4L-qZSI to meet the desired *ST* time interval naturally, eliminating the need for extra switching.
- 3DZSVM4: Similar to 3DZSVM8, but partitions the *ST* time interval into four sections within a single control cycle.
- 3DZSVM2: Divides the *ST* time interval into two portions per control period, requiring adjustments to the switching times of four switches.

In all cases, a reference voltage is generated using a series of strategically chosen switching vectors. Table 3.4 provides a detailed breakdown of the switching sequences used for each phase (*a, b, c,* and *n*) across different sectors [36].

Table 3.4 Interchanging of switching states in all sectors

Sector 1	***Sector 2***	***Sector 3***	***Sector 4***	***Sector 5***	***Sector 6***
a, b, c, n	*b, a, c, n*	*b, c, a, n*	*c, b, a, n*	*c, a, b, n*	*a, c, b, n*

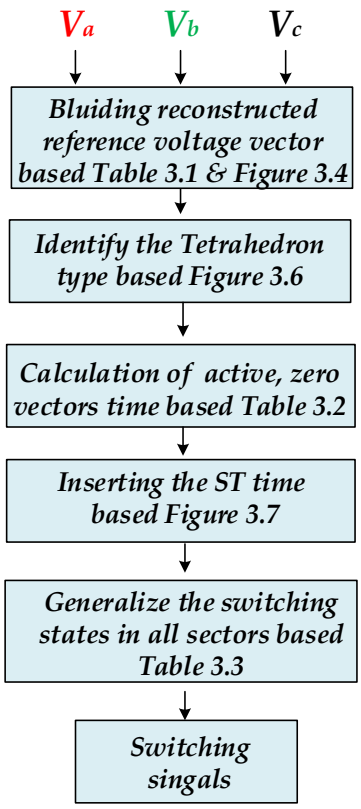


Figure 3.8. Flowchart of the proposed 3DZSVM for the 4L-qZSI

To further enhance understanding, Figure 3.8 presents a comprehensive flowchart outlining the optimized 3DZSVM method for the 4L-qZSI system. This flowchart visually depicts the step-by-step process, including calculating time intervals, determining switching sequences, and controlling inverter operation. By illustrating these intricacies, the flowchart offers valuable insight into how the 3DZSVM method is implemented within the 4L-qZSI system.

3.5 Simulation Results

To evaluate the performance of 3DZSVM for a 4L-qZSI, the simulation employed parameters defined in Table A.2. The analysis encompassed three distinct scenarios, examining the behavior of 3DZSVM under both steady-state and transient operating conditions

- Case *(C1*): Balanced peak reference voltages (V_{oa} = V_{ob} = V_{oc} = 88 V) and balanced loads (R_a = R_b = R_c = 20 Ω, L_a = L_b = L_c = 10 mH)).
- Case *(C2*): Balanced peak reference voltages (V_{oa} = V_{ob} = V_{oc} = 88 V) and unbalanced loads (R_a= 30 Ω, R_b= 10 Ω, R_c= 60 Ω, L_a=0 mH, L_b=5 mH, L_c=10 mH).
- Case *(C3*): Unbalanced peak reference voltages (V_{oa} =88 V, V_{ob} = 44 V, V_{oc} = 22 V) and balanced loads (R_a = R_b = R_c = 20 Ω, L_a = L_b = L_c =10 mH)).

For all three scenarios, the simulation maintains a constant input voltage of V_{in} = 130V and a fixed *ST* duty ratio of 0.2. With these settings, the theoretical peak voltage across the DC-link (V_{dc}) is expected to reach 216V. The load consists of an *RL* configuration connected to the inverter through an *LC* filter, as depicted in Figure 3.1. Figures 3.9 present the simulation results for the 4L-qZSI employing the proposed 3DZSVM4 technique. These results include waveforms for the DC-link voltage, inductor current, output current, output voltage, and neutral current. Simulations conducted on a 4L-qZSI using MATLAB/Simulink validate the effectiveness of the proposed modulation strategy. The results consistently demonstrate that the actual output voltages (V_a, V_b, V_c) closely track their respective reference values (V_a*, V_b*, V_c*). As expected, the peak V_{dc} reaches 216 V from an initial fixed V_{in} of 130 V. This boost is achieved with a modulation index (*M*) of 0.7. Notably, the V_{dc} voltage remains stable throughout all the simulated scenarios.

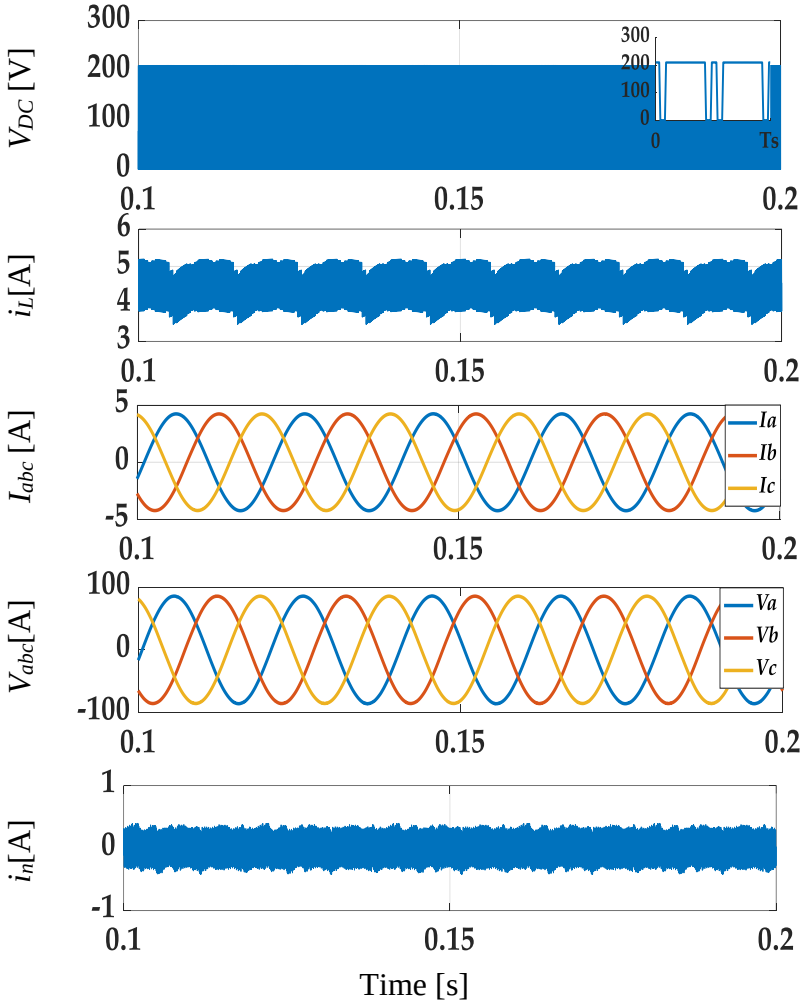


Figure 3.9: Simulation results of case C1.

Scenario C1 simulates a balanced three-phase load supplied by the 4L-qZSI. The reference peak voltage is set to 88 V, and as shown in Figure 3.9, the actual peak AC voltage successfully matches this reference. Under balanced conditions, the neutral current (the sum of the three-phase load currents) is zero, as expected. The V_{dc} exhibits a pulsating characteristic, with its peak reaching 215V during active vectors and dropping to zero during *ST* vectors. Consequently, the average current through inductor L_1 is approximately 4.5A, with a peak-to-peak ripple (Δi_{L1}) of 1A.

Scenario C2, depicted in Figure 3.10, investigates unbalanced loads. In this case, the neutral current path becomes active, flowing through the fourth leg of the inverter. Despite the unbalanced load, the output voltage successfully tracks its reference, while the output current adjusts to deliver power to the individual phases according to their respective loads.

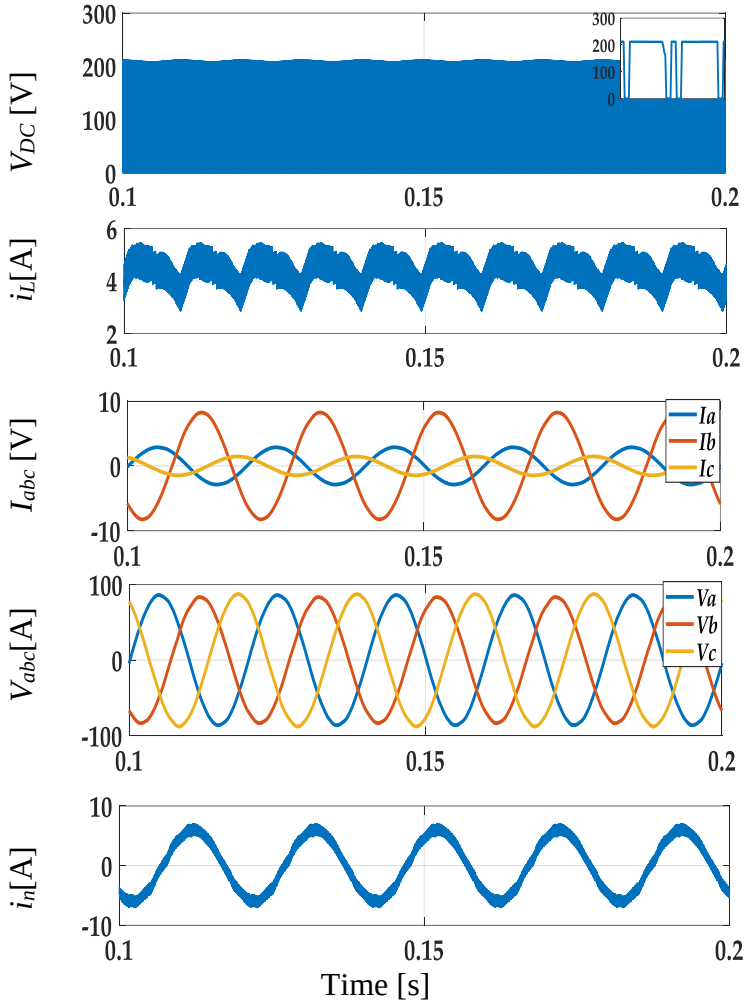


Figure 3.10 Simulation results of case C2.

Scenario C3, depicted in Figure 3.11, investigates unbalanced reference voltages. We intentionally reduced the amplitude of the reference voltage (V_{ref}) for phases (*b*) and (*c*) to 50% and 25%, respectively. As expected, the system successfully aligns the unbalanced output voltages with their corresponding reference values. This demonstrates the system's ability to regulate its output voltages accurately, even under varying reference voltages across different phases. Notably, in all three scenarios, the peak V_{dc} remains constant at 215 V due to the consistent input voltage and *ST* value of 0.2.

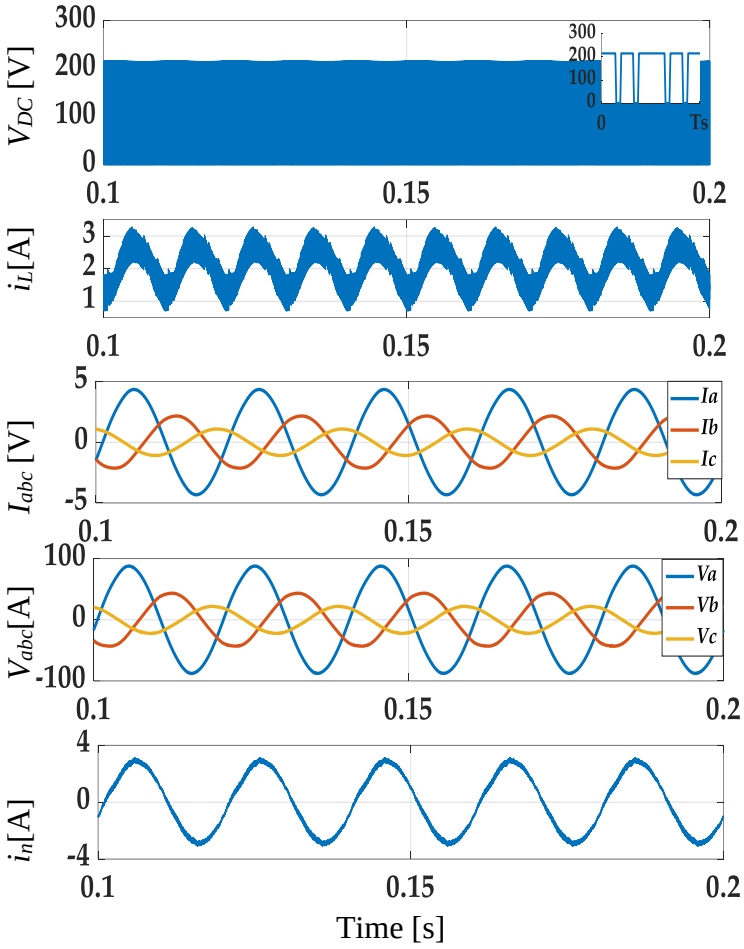


Figure 3.11. Simulation results of the steady-state analysis with unbalanced reference voltages and balanced loads.

3.6 Inductor Current Ripple Analysis

Figure 3.12 compares the inductor current of the 4L-qZSI under unbalanced load conditions (case C2) using the proposed 3DZSVM2, 3DZSVM4, and 3DZSVM8 strategies against the traditional CZPWM technique [18]. All strategies exhibit periodic fluctuations in the instantaneous inductor current ripple (Δi_{L1}) within a single fundamental cycle (equivalent to 40 ms). For instance, within one cycle, the peak Δi_{L1} values for 3DZSVM2, 3DZSVM4, 3DZSVM8, and CZPWM are 5A, 2.5A, 5.2A, and 3.5A, respectively.

The 3DZSVM4 strategy demonstrates a significant reduction in the maximum Δi_{L1} compared to 3DZSVM2 and 3DZSVM8, achieving a 49% decrease. This highlights the effectiveness of 3DZSVM4 in mitigating current ripple. Among the compared methods, 3DZSVM4 exhibits the most efficient control over current ripple magnitude, leading to smoother and more predictable system performance, especially critical for applications demanding high output stability and reliability.

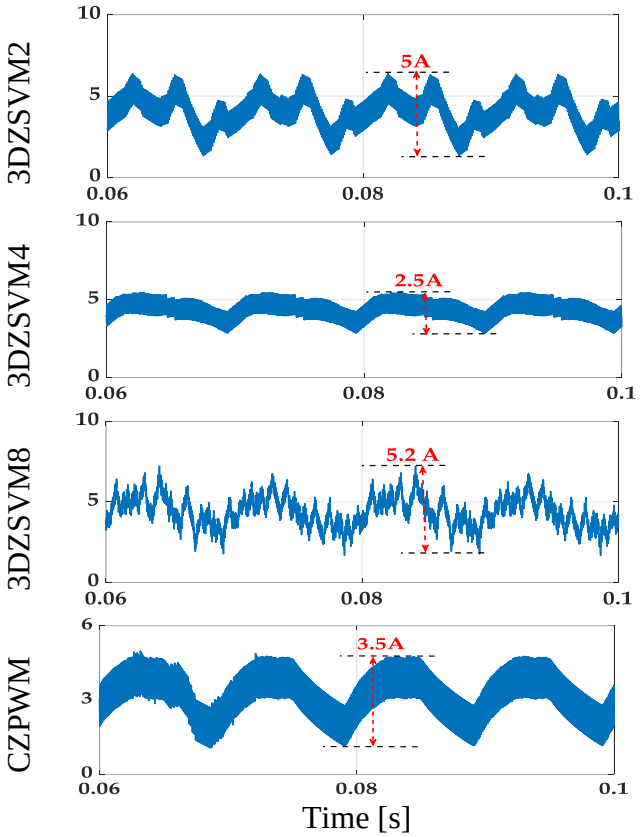


Figure 3.12. The simulation outcomes illustrate the i_{L1} behavior of the 4L-qZSI strategy throughout a single cycle in scenario C2.

3.7 Power Loss Evaluation

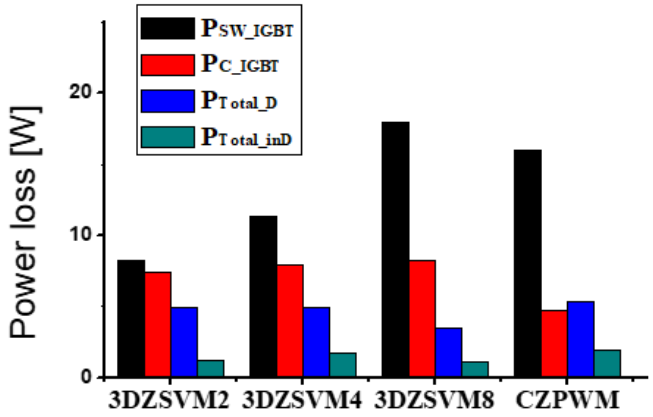
To evaluate the impact of the proposed 3DZSVM techniques on inverter efficiency, the PLECS toolbox was used to measure switching and conduction losses in the IGBTs and antiparallel diodes. IGBT and diode models were chosen as FS50R06W1E3 and VS30EPH06PbF, respectively, based on this study and references [39], [40]. Figure 3.13(a) presents a breakdown of these losses for scenario C2, comparing the conventional CZPWM technique [23] with the proposed 3DZSVM strategies. The total power loss (P_{Total}) for each technique is calculated using (3.4):

$$P_{Total} = P_{SW\text{-}IGBT} + P_{C\text{-}IGBT} + P_{Total\text{-}D} + P_{Total\text{-}inD} \quad (3.4)$$

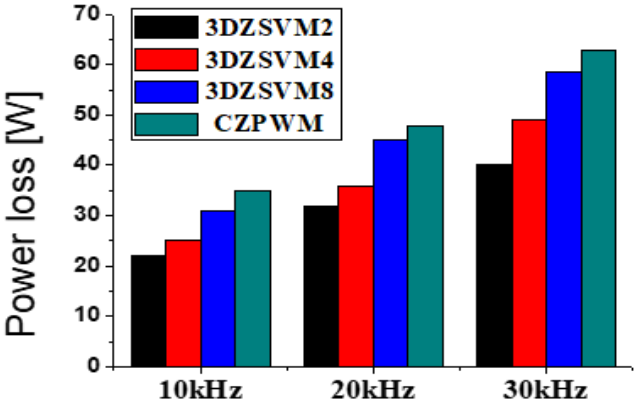
where $P_{SW\text{-}IGBT}$ and $P_{C\text{-}IGBT}$ represent the IGBT's switching and conduction losses, $P_{Total\text{-}D}$ represents the total loss in the antiparallel diode, and $P_{Total\text{-}inD}$ represents the total loss in the input diode. Finally, Figure 3.13(b) explores how varying switching frequencies affect the total power losses of the 4L-qZSI under the proposed 3DZSVM modulation strategies.

The analysis using PLECS reveals a trade-off between switching losses and total power losses with the proposed 3DZSVM techniques. As shown in Figure 3.13(a), increasing the number of *ST* divisions leads to higher switching losses. However, the 3DZSVM2

strategy achieves a lower total power loss compared to other 3DZSVM methods despite this rise. This is because 3DZSVM2 employs fewer commutations while maintaining the same average switching frequency, resulting in a better balance between these loss mechanisms. In contrast, the conventional CZPWM technique consistently exhibits the highest power loss across all switching frequencies, highlighting its lower efficiency in power utilization.



(a)



(b)

Figure 3.13. (a) Measured switching and conduction power losses distribution in the 0.6 kVA 4L-qZSI different IGBTs and input *D* under case *C2* by PLECS for CZPWM and proposed 3DZSVM strategies, (b) Total power loss of the 4L-qZSI in different switching frequencies.

3.8 Output Current and Voltage Quality

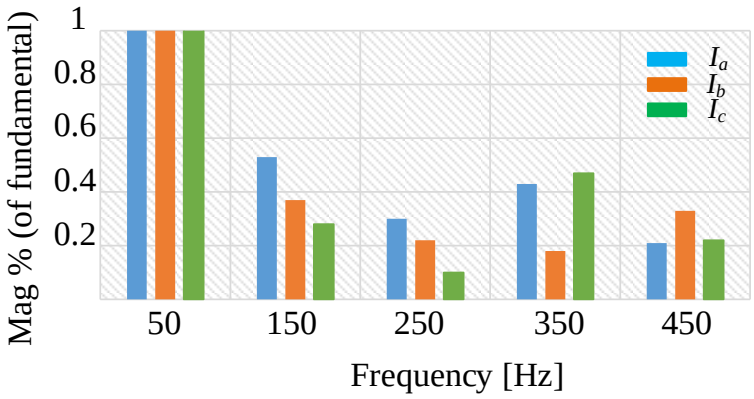
Figure 3.14 presents the THD spectrum for both the three-phase output currents and voltages under unbalanced load conditions (scenario C2). THD refers to the ratio of the combined power of all the harmonic components in a periodic waveform to the power of the fundamental frequency. Minimizing THD is crucial for maintaining high-quality power and preventing interference with other equipment connected to the grid. The THD values for the three-phase output currents in phases a, b, and c are 0.75%, 0.21%, and

0.75%, respectively. These low values indicate minimal harmonic distortion in the current waveforms.

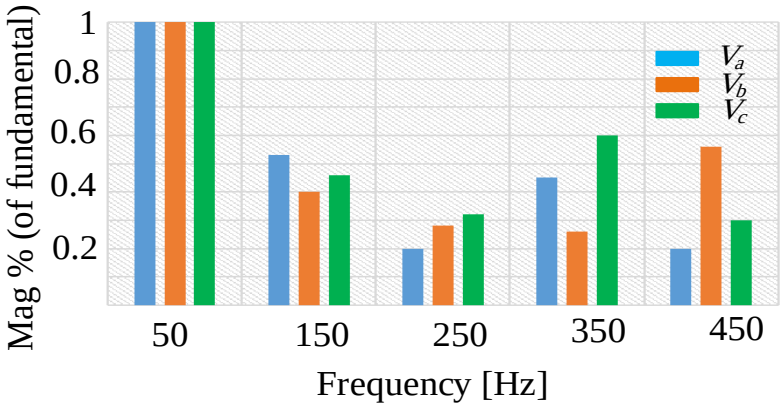
Furthermore, Table 3.5 provides details on the THD of the output voltage. As you can see, the voltage THD also falls within the acceptable limits set by the IEEE 519 standard. By achieving low THD in both currents and voltages, the system demonstrates its effectiveness in minimizing harmonic distortion. This ensures that the output power delivered by the 4L-qZSI meets the required standards for quality and performance, minimizing potential disruptions to the grid and other equipment.

Table 3.5 THD of the load voltage with the proposed 3DZSVM methods under case C2

Case	***3DZSVM2***			***3DZSVM4***			***3DZSVM8***		
	a	***b***	***c***	***a***	***b***	***c***	***a***	***b***	***c***
C1	0.79	0.72	0.7	0.63	0.68	0.69	1.5	1.4	1.3
C2	0.81	1.9	1.4	0.75	0.85	0.7	0.9	1.7	1.6
C3	1.33	3.1	3.1	1.34	3.26	3.1	4.7	7	4.5



(a)



(b)

Figure 3.14 THD spectrum at different switching frequencies for (a) output currents and (b) output load voltage.

3.9 Hardware-in-the-loop Validation Results

To validate the proposed system's real-world performance, a HIL emulation setup was constructed. This setup combines a physical microcontroller unit (MCU) with a simulated power component model. The C2000TM microcontroller LaunchPadXL TMS320F28379D kit served as the physical component, while the power circuit (including power converters and filters) was simulated within a MATLAB model (as referenced in [41], [42].

Figure 3.15 illustrates the schematic of the HIL setup. The MATLAB software acts as the virtual environment, hosting the simulated power components. The microcontroller kit, on the other hand, executes the control algorithms, specifically the proposed 3DZSVM strategy. Communication between the PC and the microcontroller kit is established through virtual serial COM ports (as described in [43], [25]. This allows MATLAB to transmit measured signals from the simulated power circuit to the kit. These signals include DC bus voltage, inductor current, capacitor voltage, load voltages, and load currents. The kit then processes these signals using the control algorithms and generates the required switching signals for the 4L-qZSI.

Figure 3.16 showcases the detailed results obtained from the HIL validation for the proposed 3DZSVM4 strategy with the 4L-qZSI under unbalanced load conditions (case C2). This figure provides valuable insights into the system's response and performance characteristics when subjected to unbalanced loads, demonstrating its operational capabilities and robustness in real-world scenarios.

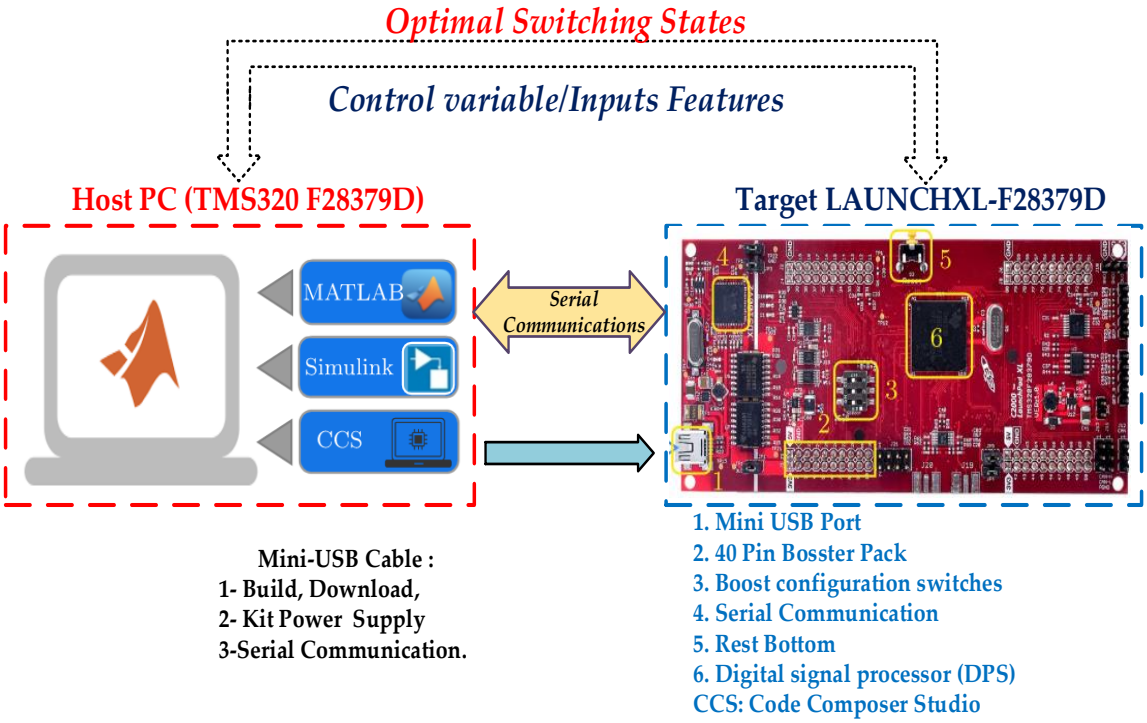


Figure 3.15. Schematic of the HIL Simulator for the Proposed System.

Scenario C2 investigates the system's behavior under unbalanced load conditions. The 4L-qZSI successfully delivers power to the unbalanced three-phase load while maintaining the desired reference voltage of 88 V peak, as shown in Figure 3.11. The output voltage closely tracks its reference, while the output current adjusts to supply each phase according to its load demand.

The DC-link voltage exhibits a pulsating characteristic, reaching a peak of 215V during active vectors and dropping to zero during shoot-through vectors. This results in an average current of approximately 4.5 A through inductor L1, with a peak-to-peak ripple of 2 A. As expected under unbalanced load conditions, the neutral current path becomes active, flowing through the inverter's fourth leg, as illustrated in Figure 3.12.

The HIL validation using the TMS320F28379D kit successfully verified the effectiveness of the proposed 3DZSVM control strategy for the 4L-qZSI under unbalanced loads (case C2). The HIL setup, which combines a physical microcontroller with a simulated power circuit model, demonstrated the practical applicability and robustness of the 3DZSVM strategy in real-world scenarios. The close agreement between the simulation and HIL results further validates the successful implementation of the proposed 3DZSVM for the 4L-qZSI.

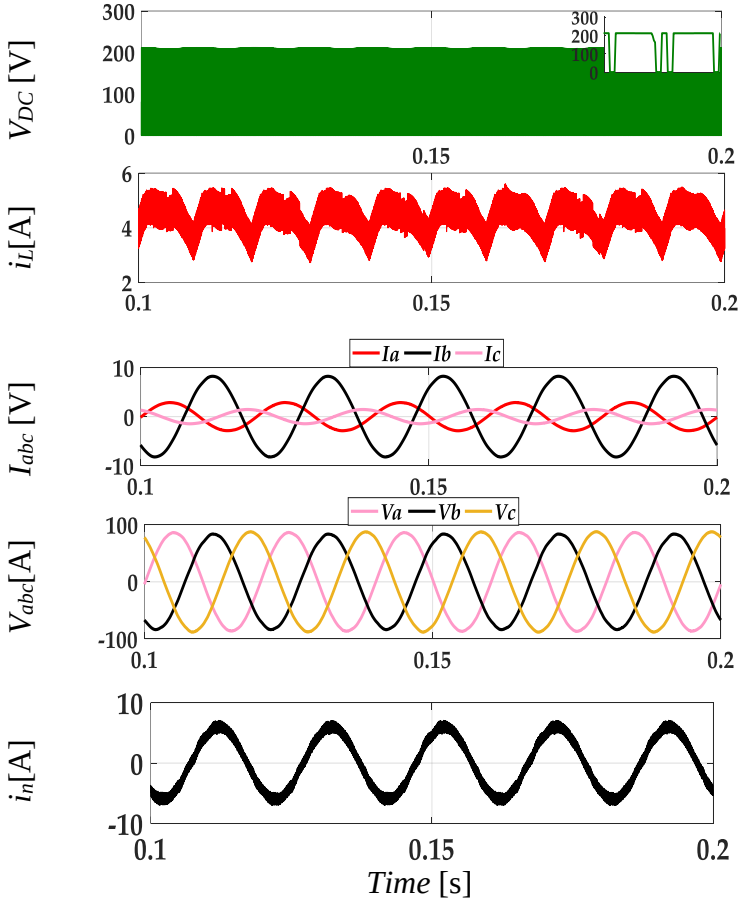


Figure 3.16. HILValidation results under case *C2*

3.10 Summary

This chapter introduces a novel 3DZSVM technique for 4L-qZSI. The proposed method, with variants named 3DZSVM2, 3DZSVM4, and 3DZSVM8, aims to improve the 4L-qZSI's performance in terms of:

- Output current quality: Reduced harmonic distortion for cleaner power output.
- Power loss: Lower power consumption for increased efficiency.
- Inductive current ripple: Minimized current fluctuations for smoother operation.

Our key innovation is the integration of the *ST* state into the 3DSVM-based ρστ coordinate system. This enhancement offers several benefits:

- Simplified calculations: Time intervals between switching vectors can be determined without trigonometric functions, even when considering the *ST* state and pulse generation.
- Reduced complexity: Calculations are primarily confined to a single sector, minimizing computational overhead.

Extensive simulations validate the effectiveness of the proposed 3DZSVM compared to the traditional CZPWM method. The results demonstrate:

- Superior steady-state performance: The 3DZSVM exhibits better overall operational characteristics.
- Reduced power loss: The system operates more efficiently with lower power consumption.
- Minimized current ripple: Inductor current fluctuations are significantly reduced.

Furthermore, HIL validation using a TMS320F28379D kit confirms the practical applicability and robustness of the 3DZSVM control strategy under unbalanced load conditions.

Potential applications:

- Stand-alone renewable energy systems: The proposed 3DZSVM is well-suited for fuel cell or photovoltaic applications operating independently, particularly when dealing with unbalanced loads.
- Improved Z-source networks: The 3DZSVM can be adapted to other advanced Z-source inverter configurations.
- Grid-connected power quality improvement: The 3DZSVM can be implemented in grid-connected systems to enhance overall power quality.

3.11 Chapter references

[1] M. E. T. Souza Junior and L. C. G. Freitas, “Power Electronics for Modern Sustainable Power Systems: Distributed Generation, Microgrids and Smart Grids—A Review,” *Sustainability*, vol. 14, no. 6, p. 3597, 2022.

[2] M. S. Hossain, N. Abboodi Madlool, A. W. Al-Fatlawi, and M. El Haj Assad, “High Penetration of Solar Photovoltaic Structure on the Grid System Disruption: An Overview of Technology Advancement,” *Sustainability*, vol. 15, no. 2, p. 1174, 2023.

[3] M. Y. Ali Khan, H. Liu, Z. Yang, and X. Yuan, “A comprehensive review on grid connected

photovoltaic inverters, their modulation techniques, and control strategies," *Energies*, vol. 13, no. 16, p. 4185, 2020.

[4] Y. Zahraoui *et al.*, "Energy management system in microgrids: A comprehensive review," *Sustainability*, vol. 13, no. 19, p. 10492, 2021.

[5] M. R. Miveh, M. F. Rahmat, A. A. Ghadimi, and M. W. Mustafa, "Control techniques for three-phase four-leg voltage source inverters in autonomous microgrids: A review," *Renew. Sustain. Energy Rev.*, vol. 54, pp. 1592–1610, 2016.

[6] J. Liang, T. C. Green, C. Feng, and G. Weiss, "Increasing voltage utilization in split-link, four-wire inverters," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1562–1569, 2009.

[7] U. Manandhar, X. Zhang, H. B. Gooi, B. Wang, and F. Fan, "Active DC-link balancing and voltage regulation using a three-level converter for split-link four-wire system," *IET Power Electron.*, vol. 13, no. 12, pp. 2424–2431, 2020.

[8] V. Khadkikar, A. Chandra, and B. Singh, "Digital signal processor implementation and performance evaluation of split capacitor, four-leg and three H-bridge-based three-phase four-wire shunt active filters," *IET Power Electron.*, vol. 4, no. 4, pp. 463–470, 2011.

[9] A. Viatkin, R. Mandrioli, M. Hammami, M. Ricco, and G. Grandi, "Ac current ripple in three-phase four-leg pwm converters with neutral line inductor," *Energies*, vol. 14, no. 5, p. 1430, 2021.

[10] D. Stracke, F. Schnabel, S. Sprunck, and M. Jung, "Efficiency comparison of three-phase four-wire inverter topologies for unbalanced and nonlinear loads," in *PCIM Europe digital days 2021; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, VDE, 2021, pp. 1–7.

[11] M. M. Fayyaz, I. M. Syed, Y. Meng, and M. N. Aman, "Comprehensive Predictive Control Model for a Three-Phase Four-Legged Inverter," *Energies*, vol. 16, no. 6, p. 2650, 2023.

[12] Y. Kwak, D. Heo, S.-P. Kim, S.-G. Song, S.-J. Park, and F. Kang, "Reliability and Economic Efficiency Analysis of 4-Leg Inverter Compared with 3-Leg Inverters," *Electronics*, vol. 10, no. 1, p. 87, 2021.

[13] M. S. Badra, S. Barkat, and M. Bouzidi, "Backstepping control of three-phase three-level four-leg shunt active power filter," *J. Fundam. Appl. Sci.*, vol. 9, no. 1, p. 274, 2017, doi: 10.4314/jfas.v9i1.18.

[14] S. Bouafia, A. Benaissa, S. Barkat, and M. Bouzidi, *Second order sliding mode control of three-level four-leg DSTATCOM based on instantaneous symmetrical components theory*, vol. 9, no. 1. Springer Berlin Heidelberg, 2018. doi: 10.1007/s12667-016-0217-5.

[15] M. Pichan and H. Rastegar, "Sliding-mode control of four-leg inverter with fixed switching frequency for uninterruptible power supply applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 8, pp. 6805–6814, 2017.

[16] K. Matsuse, N. Kezuka, and K. Oka, "Characteristics of independent two induction motor drives fed by a four-leg inverter," *IEEE Trans. Ind. Appl.*, vol. 47, no. 5, pp. 2125–2134, 2011.

[17] Y. Li, J. Anderson, F. Z. Peng, and D. Liu, "Quasi-Z-source inverter for photovoltaic power generation systems," in *2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition*, IEEE, 2009, pp. 918–924.

[18] C. J. Gajanayake, R. Teodorescu, F. Blaabjerg, D. M. Vilathgamuwa, and P. C. Loh, "Four-leg parallel Z-source inverter based DG systems to enhance the grid performance under unbalanced conditions," in *2007 European Conference on Power Electronics and Applications*, IEEE, 2007, pp. 1–10.

[19] S. Bayhan, H. Abu-Rub, and R. S. Balog, "Model predictive control of quasi-Z-source four-leg inverter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 7, pp. 4506–4516, 2016.

[20] M. Abdelrahem, U. Degmez, R. Kennel, and J. Rodriguez, "Direct model predictive control for grid-connected four-leg quasi-z-source converter under unbalanced conditions," in *PCIM Europe digital days 2020; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, VDE, 2020, pp. 1–8.

[21] S. Bayhan, M. Trabelsi, H. Abu-Rub, and M. Malinowski, "Finite-control-set model-predictive control for a quasi-Z-source four-leg inverter under unbalanced load condition," *IEEE Trans. Ind. Electron.*, vol. 64, no. 4, pp. 2560–2569, 2016.

[22] A. Bakeer, M. A. Ismeil, and M. Orabi, "A Powerful Finite Control Set-Model Predictive Control Algorithm for Quasi Z-Source Inverter," *IEEE Trans. Ind. Informatics*, vol. 12, no. 4, 2016, doi:

10.1109/TII.2016.2569527.

[23] A. Bakeer and A. A. Ahmed, "Performance evaluation of PMSM based on model predictive control with field weakening operation and bidirectional quasi Z-source inverter," in *2017 Nineteenth International Middle East Power Systems Conference (MEPCON)*, IEEE, 2017, pp. 741–746.

[24] A. Bakeer, M. A. Ismeil, A. Kouzou, and M. Orabi, "Development of MPC algorithm for quasi Z-source inverter (qZSI)," in *2015 3rd International Conference on Control, Engineering & Information Technology (CEIT)*, IEEE, 2015, pp. 1–6.

[25] H. Albalawi *et al.*, "Fractional-Order Model-Free Predictive Control for Voltage Source Inverters," *Fractal Fract.*, vol. 7, no. 6, 2023, doi: 10.3390/fractalfract7060433.

[26] A. Bakeer, M. A. Ismeil, and M. Orabi, "Modified finite control set-model predictive controller (MFCS-MPC) for quasi z-source inverters based on a current observer," *J. Power Electron.*, vol. 17, no. 3, 2017, doi: 10.6113/JPE.2017.17.3.610.

[27] J.-H. Kim and S.-K. Sul, "A carrier-based PWM method for three-phase four-leg voltage source converters," *IEEE Trans. power Electron.*, vol. 19, no. 1, pp. 66–75, 2004.

[28] S. Y. Kim, S. G. Song, and S. J. Park, "Minimum loss discontinuous pulse-width modulation per phase method for three-phase four-leg inverter," *IEEE Access*, vol. 8, pp. 122923–122936, 2020.

[29] F. Zhang and Y. Yan, "Selective harmonic elimination PWM control scheme on a three-phase four-leg voltage source inverter," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1682–1689, 2009.

[30] P. Liu, J. Xu, Y. Yang, H. Wang, and F. Blaabjerg, "Impact of modulation strategies on the reliability and harmonics of impedance-source inverters," *IEEE J. Emerg. Sel. Top. Power Electron.*, 2019.

[31] A. Abid, L. Zellouma, M. Bouzidi, A. Lashab, M. T. Boussabeur, and B. Rabhi, "A Comparative Study of Recent Discontinuous Modulation Techniques for Three-Phase Impedance Source Inverter," *SEPOC 2021*, 2021.

[32] R. Zhang, V. H. Prasad, D. Boroyevich, and F. C. Lee, "Three-dimensional space vector modulation for four-leg voltage-source converters," *IEEE Trans. power Electron.*, vol. 17, no. 3, pp. 314–326, 2002.

[33] M. Zhang, D. J. Atkinson, B. Ji, M. Armstrong, and M. Ma, "A near-state three-dimensional space vector modulation for a three-phase four-leg voltage source inverter," *IEEE Trans. Power Electron.*, vol. 29, no. 11, pp. 5715–5726, 2014, doi: 10.1109/TPEL.2013.2297205.

[34] M. Bouzidi, S. Barkat, and A. Krama, "Simplified hybrid space vector modulation for multilevel diode clamped converter," *IET Power Electron.*, vol. 13, no. 17, pp. 3861–3870, 2020, doi: 10.1049/iet-pel.2020.0529.

[35] A. Abid, A. Bakeer, L. Zellouma, M. Bouzidi, A. Lashab, and B. Rabhi, "Low Computational Burden Predictive Direct Power Control of Quasi Z-Source Inverter for Grid-Tied PV Applications," *Sustainability*, vol. 15, no. 5, p. 4153, 2023.

[36] M. Bouzidi, S. Barkat, and A. Krama, "New Simplified and generalized Three-Dimensional Space Vector Modulation Algorithm for Multilevel Four-Leg Diode Clamped Converter," *IEEE Trans. Ind. Electron.*, vol. 0046, no. c, pp. 1–1, 2020, doi: 10.1109/tie.2020.3026298.

[37] X. Li, Z. Deng, Z. Chen, and Q. Fei, "Analysis and simplification of three-dimensional space vector PWM for three-phase four-leg inverters," *IEEE Trans. Ind. Electron.*, vol. 58, no. 2, pp. 450–464, 2010.

[38] Y. Liu, B. Ge, H. Abu-Rub, and F. Z. Peng, "Overview of space vector modulations for three-phase Z-source/quasi-Z-source inverters," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 2098–2108, 2013.

[39] A. Bakeer, A. Chub, Y. Shen, and A. Sangwongwanich, "Reliability analysis of battery energy storage system for various stationary applications," *J. Energy Storage*, vol. 50, p. 104217, 2022.

[40] P. Liu, J. Xu, M. Sun, J. Yuan, and F. Blaabjerg, "New discontinuous space vector modulation strategies for impedance-source inverter with superior thermal and harmonic performance," *IEEE Trans. Ind. Electron.*, vol. 69, no. 12, pp. 13079–13089, 2022.

[41] A. Bakeer, I. S. Mohamed, P. B. Malidarreh, I. Hattabi, and L. Liu, "An Artificial Neural Network-Based Model Predictive Control for Three-Phase Flying Capacitor Multilevel Inverter," *IEEE Access*, vol. 10, no. May, pp. 70305–70316, 2022, doi: 10.1109/ACCESS.2022.3187996.

[42] I. S. Mohamed, "Implementation of model predictive control for three-phase inverter with output LC filter using DSP." Control Engineering, Faculty of Engineering, Cairo University, 2014.

[43] S. A. Zaid *et al.*, "From MPC-Based to End-to-End (E2E) Learning-Based Control Policy for Grid-Tied 3L-NPC Transformerless Inverter," *IEEE Access*, vol. 10, pp. 57309–57326, 2022, doi: 10.1109/ACCESS.2022.3173752.

Chapter 4

Predictive Direct Power Control of qZSI for Grid-Tied PV Application

This chapter introduces a simplified predictive direct power control (PDPC) strategy for a grid-tied qZSI. This control method leverages a predictive control structure to extract maximum power from the connected PV source. It also manages the delivered grid power to compensate the reactive power and as well as ensures grid stability.

A key innovation is the development of a predictive power model for the qZSI. This model enables the PDPC to operate with a fixed switching frequency and eliminates the need for weighting factors. Additionally, a simplified ZSVM technique is employed. This method selects and applies three appropriate switching vectors during each switching period using pre-calculated dwell times. Notably, the required vectors are determined solely from one sector of the space vector diagram, while incorporating information from all other sectors. This approach significantly reduces the computational burden of the control scheme.

The effectiveness of the proposed control strategy is validated through simulation results and a comparative study. The results demonstrate the qZSI's capability to:

- Track and generate maximum power from the PV source with fast dynamics.
- Maintain the desired AC voltage.
- Achieve superior tracking of active and reactive power references with minimal power ripple.
- Comply with the IEEE-519 standard for grid current harmonics.

Furthermore, the usability and effectiveness of the proposed simplified PDPC are confirmed through experimental validation using a HIL emulator and a Texas Instruments C2000™ microcontroller LaunchPadXL TMS320F28379D kit.

4.1 Overview

Effective control strategies are crucial for grid-connected converters (GCCs) as they directly impact power quality. Consequently, significant research has been dedicated to developing control strategies for grid-connected systems [1],[2]. Literature explores various qZSI control methods, encompassing linear and non-linear approaches in synchronous, stationary [3]. However, these methods often rely heavily on the performance of the inner current loop, which utilizes proportional-integral (PI) controllers. Tuning PI controllers for decoupling can be complex, and limitations exist in achieving error-free adjustments [4]. Additionally, the bandwidth of the phase-locked loop (PLL) for synchronization can also impact overall performance [5].

Direct power control (DPC) offers an attractive alternative control method due to its simplicity, ability to achieve low current distortion, and strong dynamic response [6].Traditional DPC employs a power hysteresis comparator and a switching vector table for voltage vector selection. It directly controls active and reactive power without requiring an inner current loop or a pulse-width modulation (PWM) block [7]. However, the use of hysteresis comparators for power control introduces drawbacks such as increased power ripple, variable switching frequency, and a wider range of harmonic content, which complicates line filter design.

In recent years, model predictive control (MPC) has emerged as a popular choice for power converters due to its inherent advantages: simplicity, flexibility, and the ability to seamlessly integrate control constraints [8]–[12].

While decoupling between active and reactive power control has been explored [13], it often requires introducing weighting factors in the cost function, which can lead to increased output power ripple [13]. Other studies propose improvements like enhanced MPPT algorithms for better current quality [14], but these can introduce model complexity. Although model predictive control for dual-mode ZSI operation has been proposed [15], it suffers from variable switching frequency. Similarly, attempts to eliminate weighting factors for reduced computational burden come at the cost of significant power ripple [16].

However, the traditional MPC offers advantages, three limitations hinder its effectiveness. Firstly, the variable switching frequency inherent to MPC generates significant current ripple, which complicates filter design. Secondly, selecting weighting factors is a challenge, often requiring a trial-and-error approach guided by complex theoretical considerations [17], [18]. Finally, traditional MPC relies on computationally expensive continuous optimization to find the optimal control vector.

Addressing the limitations of traditional MPC, PDPC emerges by combining MPC with instantaneous power theory. Compared to DPC, PDPC leverages cost function minimization to ensure optimal vector selection, prioritizing power ripple reduction [19]. Additionally, PDPC-SVM, as detailed in [20], is employed to mitigate the variable frequency inherent to

PDPC. This approach offers several advantages, including: i) Harmonic current mitigation ii) Power factor correction, iii) Active power injection, vi) Low switching frequency operation [21].

In the qZSI, the *ST* action involves simultaneously turning on the upper and lower switches in the same leg. The ZSVM techniques, like the ZSVM6 strategy [22], achieve *ST* by dividing the designated *ST* time equally and inserting those segments strategically within the switching cycle, leaving the active switching states unchanged. This division reduces the charge/discharge intervals, leading to smaller inductor current ripples. ZSVM techniques can be further categorized based on the number of divisions used for the *ST* duration: ZSVM1 (one division), ZSVM2 (two divisions), and so on, up to ZSVM6 (six divisions) [23]. To reduce complexity and computational burden, a simplified ZSVM6 approach for the qZSI was proposed. This method utilizes only one sector in the voltage space vector to calculate all the necessary switching sequences for the ZSVM strategy.

This chapter proposes a simplified PDPC strategy specifically designed for grid-tied qZSI. This approach reduces computational burden by eliminating the need for complex cost function calculations. The control strategy efficiently selects the optimal switching vector while minimizing computational requirements. To control the active and reactive power injected into the grid, a simplified ZSVM technique is introduced. This technique eliminates the need for weighting factor calculations by using a PI linear controller with an MPPT unit for optimal operation. The simplified PDPC offers two key benefits: reduced grid current/power ripple and significantly decreased computation time.

This chapter is organized as follows. The core of this work, the proposed simplified PDPC algorithm for the qZSI, is presented in detail in Section 4.2. Section 4.3 explores the simplified space vector modulation technique. Sections 4.4 and 4.5 illustrate the simulation results and conduct a comparative study to highlight the effectiveness of the proposed approach. To validate the practical applicability of the method, Section 4.6 presents a Hardware-in-Loop (HIL) simulation. Finally, Section 4.7 concludes the chapter by summarizing the key findings.

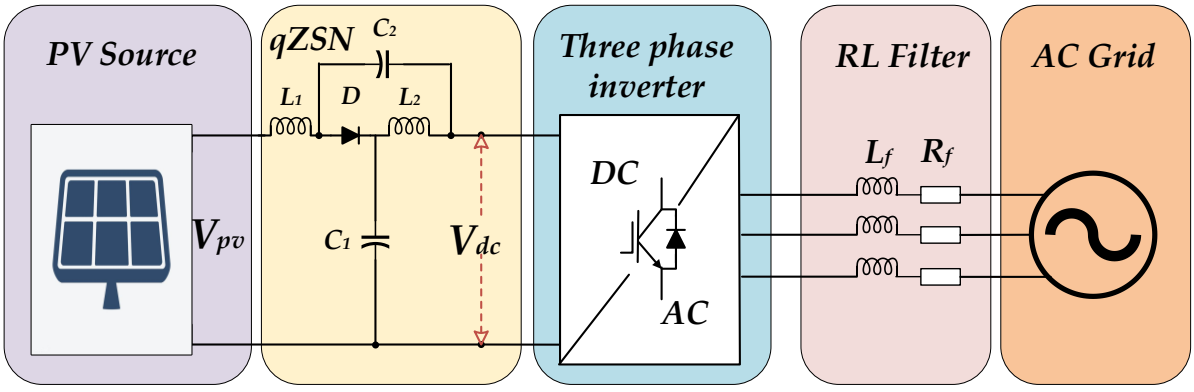


Figure 4.1. Typical configuration of a grid-connected three-phase qZSI.

4.2 Description of Simplified PDPC Approach

The control method, as shown in Figure 4.1, integrates the qZSI into the grid and ensures the PV system operates at the Maximum Power Point (MPP). It comprises several components: instantaneous power control, model predictive controller, MPPT control, *ST* segment ZSVM strategy, and PI regulator. The control structure consists of two main parts. The first is the DC circuit control in the PV source, where MPPT is applied.

4.2.1 DC Side Control

To find the optimal operating point (MPP), the perturb and observe (P&O) method is used, as illustrated in Figure 4.2. The P&O algorithm searches for the V_{MPP} (voltage at the MPP) by comparing it with the measured voltage of the PV array. A PI controller then regulates the PV voltage in a closed loop, adjusting the duty cycle of the switching element (*ST*) to achieve the desired PV voltage reference.

$$D = k_P\left(V_{PV}^{*} - V_{PV}\right) + k_I\int_0^t\left(V_{PV}^{*} - V_{PV}\right)dt \tag{4.1}$$

While the integral and proportional parameters, respectively, are denoted by k_P and k_I. The PV voltage tracking inaccuracy is according to:

$$E = V_{PV}^{*} - V_{PV} \tag{4.2}$$

Usually, the transfer function of the PI controller is:

$$G_{PI} = \frac{D}{E} = \frac{k_P p + k_I}{p} \tag{4.3}$$

The gains k_P and k_I of the PI regulator are determined using the Bode plot approach.

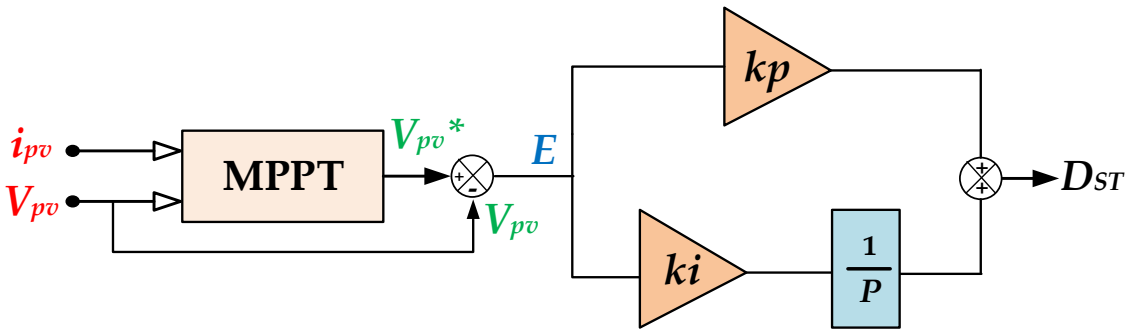


Figure 4.2. Output PV voltage loop.

4.2.2 Mathematical Modeling of the PDPC

The second part focuses on controlling the injected active and reactive power to desired values. To achieve this, the proposed simplified PDPC calculates the average voltage vector of the qZSI ($V_{\alpha\beta}$) at each sampling time using a predictive control algorithm. The inputs to this algorithm are the instantaneous active and reactive power, their reference values, and the grid voltage vector ($e_{\alpha\beta}$) (see Figure 4.4). For constant switching frequency and reduced

computation time, a simplified ZSVM approach is employed to generate the desired average voltage vector ($V_{\alpha\beta}$) at the qZSI's output.

In power system control, prediction plays a crucial role. It allows us to anticipate the control variables needed during the next sampling period to achieve the desired performance. In this context, a prediction model can be developed using active and reactive power as the key controllable variables. The following equations describe these power components in a stationary reference frame (α, β) for a balanced three-phase system:

$$\begin{bmatrix} P \\ q \end{bmatrix} = \begin{bmatrix} e_\alpha & e_\beta \\ e_\beta & -e_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{4.4}$$

When the T_S is supposed to be small in relation to the power-source voltage period, the components of e are considered to be constant across the T_S *(e(k + 1) = e(k)).*

Finally, the variation in active and reactive powers during two sequential sampling times can be interpreted as follows:

$$\begin{bmatrix} P(k+1)-P(k) \\ q(k+1)-q(k) \end{bmatrix} = \begin{bmatrix} e_\alpha(k) & e_\beta(k) \\ e_\beta(k) & -e_\alpha(k) \end{bmatrix} \begin{bmatrix} i_\alpha(k+1)-i_\alpha(k) \\ i_\beta(k+1)-i_\beta(k) \end{bmatrix} \tag{4.5}$$

Figure 4.1 shows that the qZSI is connected to the grid via an *RL* filter. The system's function at the point of common coupling (PCC) is defined as:

$$V_{abc} = Ri_{abc} + L\frac{di_{abc}}{dt} + e_{abc} \tag{4.6}$$

where V_{abc} is the output qZSI voltage, i_{abc} is the current injected into the grid through the *RL* filter, and e_{abc} is the PCC voltage. Clarke's transformation of (4.6) gives:

$$L\frac{d}{dt}\begin{bmatrix} i_\alpha(t) \\ i_\beta(t) \end{bmatrix} = \begin{bmatrix} e_\alpha(t) \\ e_\beta(t) \end{bmatrix} - \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} - R\begin{bmatrix} i_\alpha(t) \\ i_\beta(t) \end{bmatrix} \tag{4.7}$$

By neglecting the effect of the resistance R_f, the discretization of (4.7) is given as:

$$\begin{bmatrix} i_\alpha(k+1)-i_\alpha(k) \\ i_\beta(k+1)-i_\beta(k) \end{bmatrix} = \frac{T_S}{L_f}\left(\begin{bmatrix} e_\alpha(k) \\ e_\beta(k) \end{bmatrix} - \begin{bmatrix} V_\alpha(k) \\ V_\beta(k) \end{bmatrix}\right) \tag{4.8}$$

By replacing (4.8) in (4.7), the variation of active and reactive power in one T_S is obtained as follows:

$$\begin{bmatrix} P(k+1)-P(k) \\ q(k+1)-q(k) \end{bmatrix} = \frac{T_S}{L_f}\begin{bmatrix} e_\alpha(k) & e_\beta(k) \\ e_\beta(k) & -e_\alpha(k) \end{bmatrix}\left(\begin{bmatrix} e_\alpha(k) \\ e_\beta(k) \end{bmatrix} - \begin{bmatrix} V_\alpha(k) \\ V_\beta(k) \end{bmatrix}\right) \tag{4.9}$$

Based on the control objective of PDPC by forcing the active and reactive power to be equal to their reference values at the next sampling instant. Thus,

$$\begin{bmatrix} P(k+1) \\ q(k+1) \end{bmatrix} = \begin{bmatrix} P^*(k+1) \\ q^*(k+1) \end{bmatrix} \tag{4.10}$$

By substituting (4.9) in (4.10), the V_α and V_β reference voltage vectors are calculated as:

$$\begin{bmatrix} V_\alpha(k) \\ V_\beta(k) \end{bmatrix} = \begin{bmatrix} e_\alpha(k) \\ e_\beta(k) \end{bmatrix} - \frac{L_f}{T_S \left\| e_{\alpha\beta} \right\|^2}\begin{bmatrix} e_\alpha(k) & e_\beta(k) \\ e_\beta(k) & -e_\alpha(k) \end{bmatrix}\begin{pmatrix} P^*(k+1)-P(k) \\ q^*(k+1)-q(k) \end{pmatrix} \tag{4.11}$$

To achieve unity power factor in the grid-tied qZSI, the reactive power reference is set to zero ($q^* = 0$). As illustrated in Figure 4.4, the desired active power (P^*) is obtained by

multiplying the PV current (i_{PV}) with the PV voltage (V_{PV}). Based on the linear approximation depicted in Figure 4.3, the predicted value of $P^*(k+1)$ can be expressed as follows

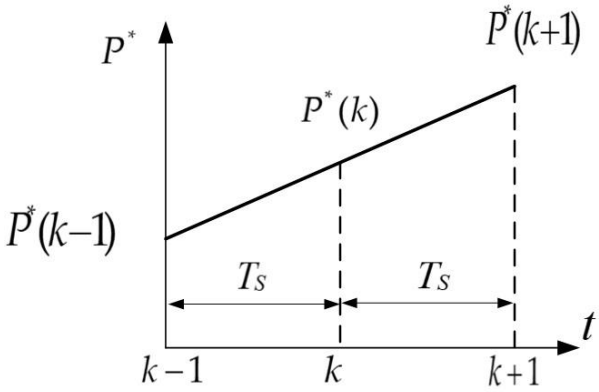


Figure 4.3. Predictive value estimation of reference active power.

$$\begin{bmatrix} P^*(k+1) \\ q^*(k+1) \end{bmatrix} = \begin{bmatrix} 2P^*(k) - P^*(k-1) \\ q^*(k) \end{bmatrix} \tag{4.12}$$

By using (4.11) and (4.12), the average control vector to be applied during the sampling period is obtained by the following Equation:

$$\begin{bmatrix} V_\alpha(k) \\ V_\beta(k) \end{bmatrix} = \begin{bmatrix} e_\alpha(k) \\ e_\beta(k) \end{bmatrix} + \frac{L_f}{T_s \left\| e_{\alpha\beta} \right\|^2} \begin{bmatrix} e_\alpha(k) & e_\beta(k) \\ e_\beta(k) & -e_\alpha(k) \end{bmatrix} \begin{pmatrix} \Delta P^*(k) + \varepsilon_p(k) \\ \varepsilon_q(k) \end{pmatrix} \tag{4.13}$$

The actual active and reactive power measuring errors are $\varepsilon_p(k)$ and $\varepsilon_q(k)$, respectively, where $\Delta P^*(k)$ represents the actual variation in active power reference level given by:

$$\Delta P^*(k) = P^*(k) - P^*(k-1) \tag{4.14}$$

The qZSI relies on PV panels as its power source. The MPPT control ensures these panels consistently operate at their MPP, delivering the highest possible output. Consequently, the reference power injected into the grid (P^*) represents the maximum power harvested from the PV panels at any given time. The following section delves deeper into this modulation technique.

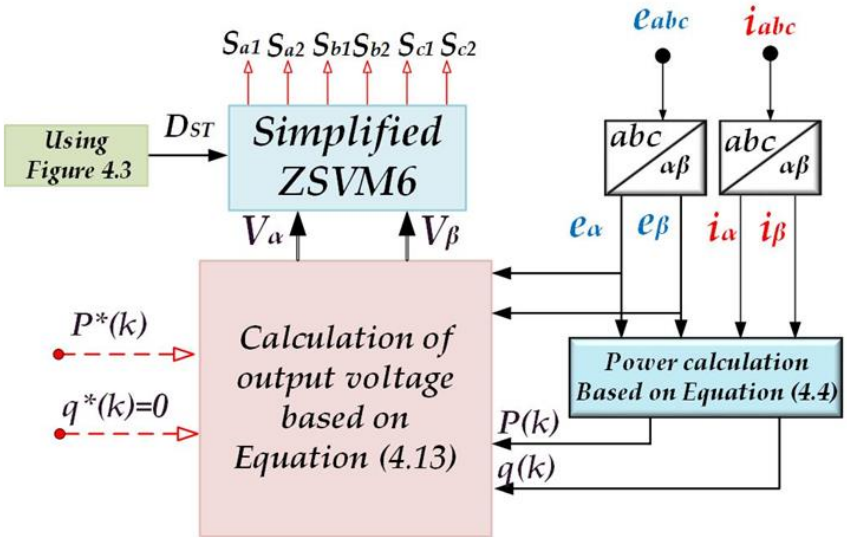


Figure 4.4. The control diagram of the proposed simplified PDPC.

4.3 The Simplified Space Vector Modulation

The traditional SVM method for a three-phase, two-level VSI utilizes eight switching vectors to create a hexagon, as shown in Figure 4.5. The ZSVM approach for the qZSI incorporates all these vectors, along with an additional *ST* zero state. The *ST* interval coincides with the zero vector of the traditional SVM, so its presence doesn't impact inverter operation. The switching times for the sequences in the qZSI's SVM procedure can be calculated as

$$\begin{cases} T_1 = M.T_{Sw}\sin[\pi/3-\theta+(i-1)\pi/3] \\ T_2 = M.T_{Sw}\sin[\theta-(i-1)\pi/3] \\ T_0 = T_{Sw}-T_1-T_2 \end{cases} \tag{4.15}$$

where i = 1, 2,…, 6 denotes the i^{th} sector, T_{sw} signifies the switching period, T_1 and T_2 represent the durations in time between two neighboring active vectors V_i and V_{i+1}, respectively, T_0 signifies the time interval of the zero vector, which includes the zero vector V_0, and the *ST* vector V_{sh}. V_{ref} denotes the oriented angle of the voltage reference vector the modulation index is defined as $M = \sqrt{3}V_{ref}/V_{DC}$.

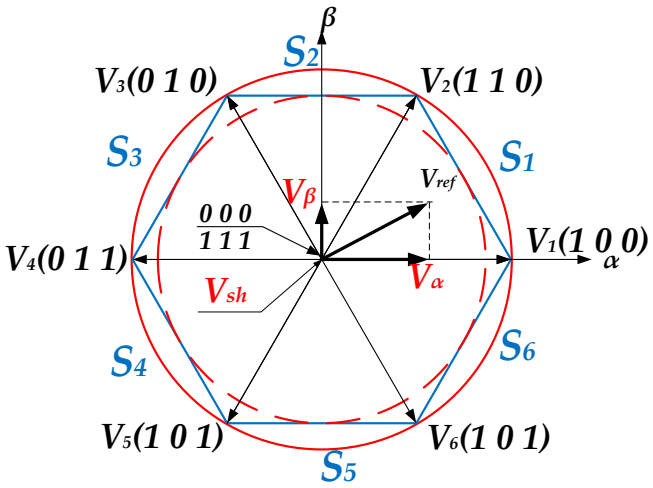


Figure 4.5. Voltage space vector for ZSVM.

Building on the concept of simplified SVM for three-phase multilevel inverters introduced in [24], which reduces complexity and computation time by using a single sector, this chapter proposes a novel simplified ZSVM strategy for grid-tied qZSI. This approach aims to achieve low computational burden and minimize hardware and software complexity.
The proposed ZSVM strategy is implemented in six key steps:

1. New voltage reference vector calculation;
2. Sector number identification;
3. Duration times calculation;
4. Pulse generation with *ST* state insertion.

4.3.1. Calculations of the New Reference Voltage Vector

To simplify the calculation, the proposed ZSVM algorithm generates a new reference voltage vector $U_{ref} = [U_a, U_b, U_c]^t$ that turns in the first sector and collects all details from the original reference voltage vector $V_{ref} = [V_a, V_b, V_c]^t$ in the other sectors. In Figure 4.6, V_{ref} rotates counterclockwise and traverses all sectors of the space vector plan. As a result, the triangle in the first sector is repeated in the remaining sectors. This similarity is based on the ability to shift the phase directions of the switching states during the first sector to conclude all the switching states for the other sectors. Hence, even if the proposed U_{ref} is only created to rotate in the first sector, the direction of its rotation is also determined by the location of V_{ref}.

Assuming that U_{ref} maintains the same triangle order as V_{ref} in all sectors, its rotation must be in the following direction (see Figure 4.6):

- V_{ref} is in an odd sector (1, 3, and 5) if rotated counterclockwise;
- V_{ref} is in an even sector (2, 4, and 6) if rotated clockwise.

With straightforward instructions, U_{ref} can be generated in the *abc* frame. Table 4.1 summarizes the selection of the *abc* components of U_{ref}, which depends on V_{ref} components and the number of sectors.

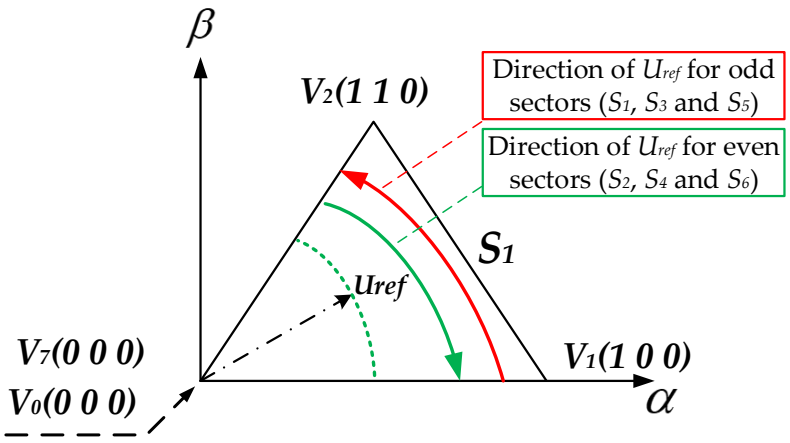


Figure 4.6. The orientation of the new vector U_{ref} in the first sector.

Table 4.1. Selection of the proposed U_{ref} elements.

	S_1	S_2	S_3	S_4	S_5	S_6
U_a	V_a	V_b	V_b	V_c	V_c	V_a
U_b	V_b	V_a	V_c	V_b	V_a	V_c
U_c	V_c	V_c	V_a	V_a	V_b	V_b

In the *abc* coordinates scheme, Figure 4.7 depicts the components of the old reference V_{ref} and proposed U_{ref}.

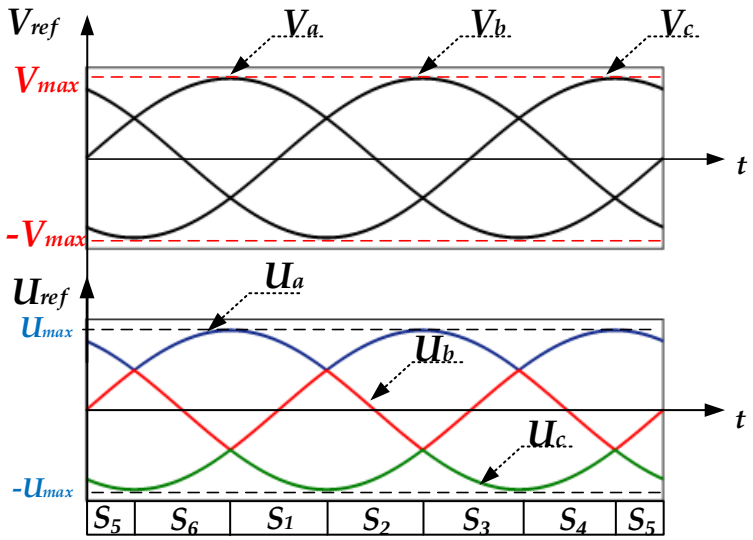


Figure 4.7. Components of V_{ref} and U_{ref} in abc coordinates.

4.3.2. Identification of the Sector Number

The sector number containing V_{ref} is required to construct U_{ref}. As a result, Table 4.2 defines the selected strategy based on an easy comparison of the elements of U_{ref} in *abc* coordinates.

Table 4.2. Identification of a sector number.

Condition	Sector Number
Va > *Vb* > *Vc*	1
Va > *Vc* > *Vb*	6
Vb > *Va* > *Vc*	2
Vb > *Vc* > *Va*	3
Vc > *Vb* > *Va*	4
Vc > *Va* > *Vb*	5

4.3.3. Calculation of Duration Time

To calculate the on-duration time intervals of each switching vector, the average value principle is used and is obtained as follows:

$$\begin{cases} V_1 t_1 + V_2 t_2 + V_0 t_0 = V_{ref} T_{Sw} \\ t_1 + t_2 + t_0 = T_{Sw} \end{cases} \tag{4.16}$$

where t_1, t_2, and t_0 are the corresponding on-duration time interval for the three switching vectors next to the reference voltage vector, V_1, V_2, and V_0, respectively. The (4.16) is then converted into $\alpha\beta$ coordinates as follows:

$$\begin{bmatrix} V_{1\alpha} & V_{2\alpha} & V_{0\alpha} \\ V_{1\beta} & V_{2\beta} & V_{0\beta} \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} t_1 \\ t_2 \\ t_0 \end{bmatrix} = \begin{bmatrix} V_{\alpha ref} \\ V_{\beta ref} \\ T_{sw} \end{bmatrix} \tag{4.17}$$

Finally, the on duration can be calculated using (4.17) based on the voltage reference in $\alpha\beta$ coordinates generated by the PDPC.

4.3.4. Pulses Generation

The switching operation of the qZSI using the ZSVM includes one additional *ST*, zero vectors, and six active voltage vectors. To create the *ST* state for the ZSVM of qZSI, one of the three-phase legs, *a*, *b*, and *c*, are in a short circuit each switching period. The preferred total *ST* duration is divided into six time during each switching period. One-phase *ST* reduces switching losses across the whole switching period by assuming that only one bridge leg can be altered at a time. Figure 4.6 shows the corresponding voltage space vectors of the qZSI in an $\alpha\beta$ projection. The switching sequences of the proposed ZSVM6 algorithm in the first sector are detailed in Figure 4.8 to facilitate switching state selection. Thus, for each sector, the qZSI reference voltage vector becomes:

$$V_{ref} = V_1 \frac{T_1}{T_{Sw}} + V_2 \frac{T_2}{T_{Sw}} + V_0 \frac{T_0}{T_{Sw}} + V_{sh} \frac{T_{sh}}{T_{Sw}} \tag{4.18}$$

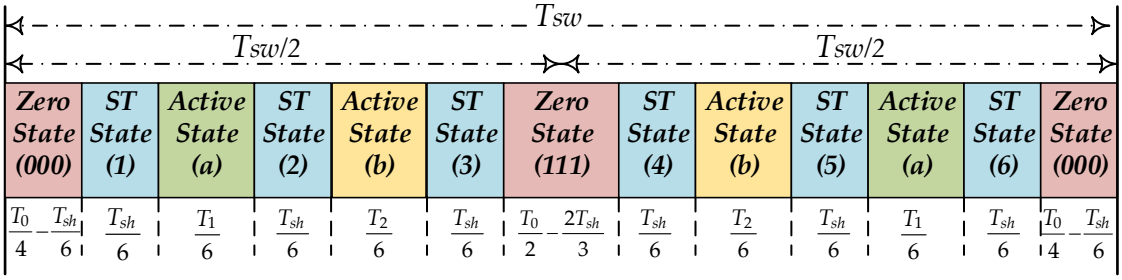


Figure 4.8 Switching pattern for ZSVM6.

Therefore, the reference voltage is generated using the three adjacent switching vectors. The main objective is to reduce the harmonic content of the output voltage/current by arranging the switching transitions. Table 4.3 summarizes the adopted interchanging between phases *a*, *b*, and *c* in all sectors.

Table 4.3. Interchanging switching states in all sectors.

Sector 1	*Sector 2*	*Sector 3*	*Sector 4*	*Sector 5*	*Sector 6*
a, b, c	*b, a, c*	*b, c, a*	*c, b, a*	*c, a, b*	*a, c, b*

Lastly, Figure 4.9 shows the flow diagram of the proposed simplified ZSVM6 algorithm for the grid-tied qZSI. The proposed simplified PDPC generates the voltage vector reference V_α and V_β, and utilized Table 4.2 to create the new U_{ref} for reducing the calculation. The indentation of the sector number is necessary to calculate the vector duration and to generalize in all sectors, Table 4.3 illustrates that.

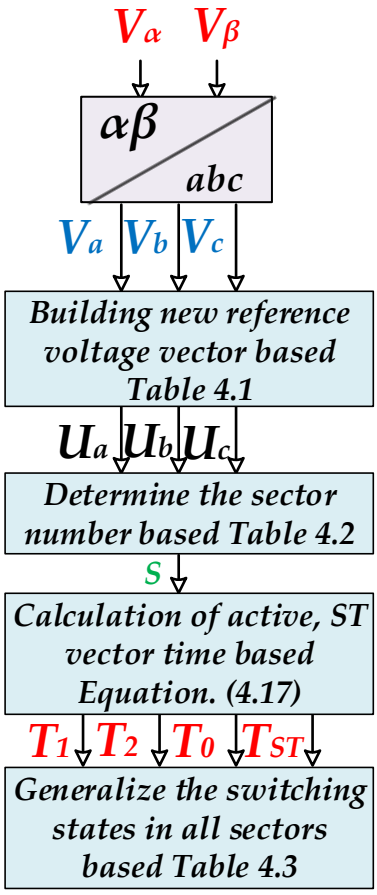


Figure 4.9: Flow diagram of the proposed simplified ZSVM6.

4.4 Simulation Results

MATLAB/Simulink is used to simulate the model of the three-phase grid-tied qZSI fed by a PV power system to evaluate the performance of the simplified PDPC method and control structure, as shown in Figure 4.1. The PV panel's parameters under the standard test conditions (STC) are shown in Table A.3. To achieve the required *ac* voltage level, four PV panels were interconnected in a series in each PV string. The electrical system parameters are listed in Table A.4. The results are presented in Figures 4.10–18 and have been validated for the abovementioned criteria. The system's operation under the dynamic response can be tested under different meteorological conditions. The studied conditions are 1000 W/m^2, 800 W/m^2, and 500 W/m^2, respectively.

As seen in Figure 4.10, the MPPT operated by P&O precisely follows the theoretical reference. It tracks the maximum voltage with excellent stability and low oscillation. Despite the quick change in irradiation, the panels maintain their maximum output voltage (around 185 V). As seen in Figures 4.11 and 4.12, the suggested simplified PDPC can effectively adjust to step variations in the power references, and the maximum output power of the PV source was transferred to the grid with a small active power ripple. As a result, in Figure 4.13, maintaining reactive power near zero and ensuring that the qZSI is unaffected by changes in active power, allowing the converter to operate at the unity power factor.

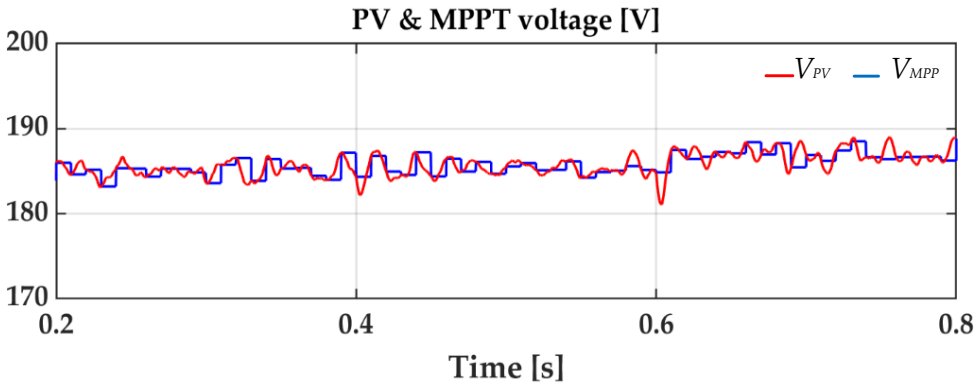


Figure 4.10: The measured and generated output PV voltage.

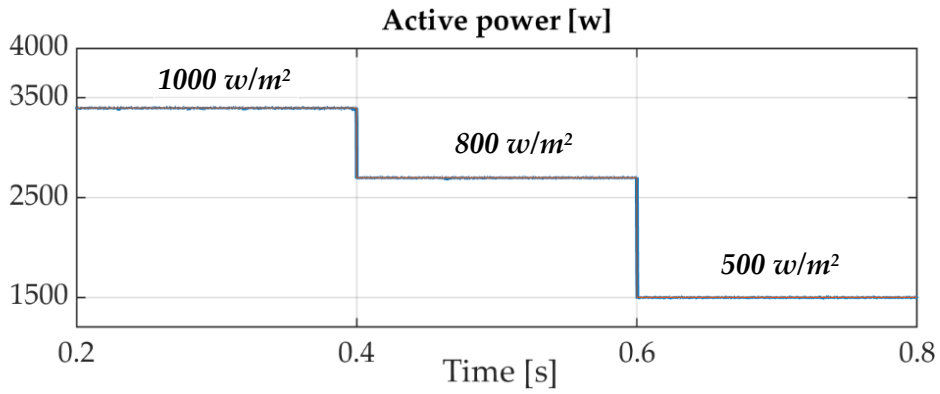


Figure 4.11: Output active power with a different level of irradiation.

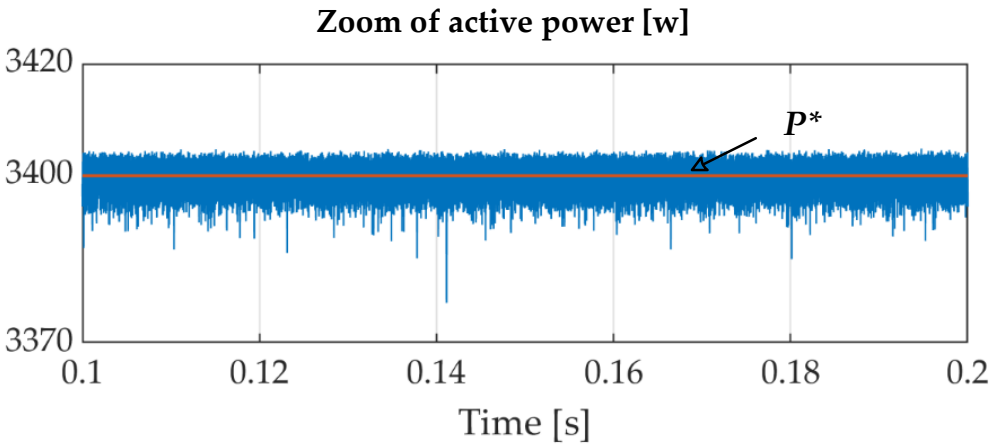


Figure 4.12: Zoom of view in the active output power under 1000 W/m^2.

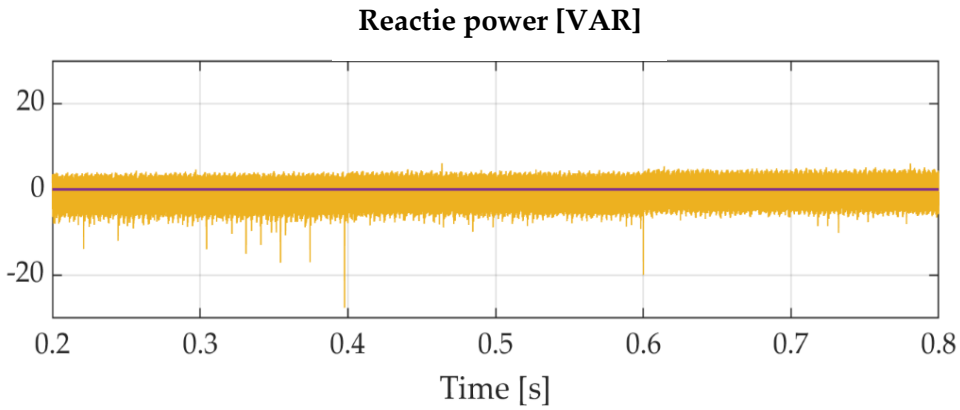


Figure 4.13: Reactive power under different levels of solar irradiation.

It is shown in Figure 4.14, the *ST* duty cycle is controlled to maintain a DC-link peak voltage value during all the changing in the irradiation and produces a pulse voltage waveform since, in the *ST* state, the dc-link voltage is zero, while in the active state, the peak dc-link voltage value around 250V. As shown in Figure 4.15, the V_{C1} was continuously followed at 220V during the transient situation, exhibiting the dynamic functionality and efficiency of the proposed control. Figure 4.16 shows the inductive current waveform during the irradiation changes. It can be seen that the i_{L1} decreases from 20A to 15A at 0.4s and decreases from 15A to 8A at 0.6s. However, we can observe the double frequency comment in the inductive current curve duo to the used one leg for the qZSI for *ST* state. Therefore, the dynamic performance of the qZSI was unaffected by the inductive current ripples.
The V_a and i_a, as presented in Figure 4.17, are in phase, and the output currents are nearly sinusoidal and fluctuate smoothly. During the irradiation changes, where it can be quickly adjusted without causing overshoot or undershoot currents.
Figure 4.18 illustrates the grid-tied qZSI's test results in a 1000 W/m^2 steady state, where the current injected into the grid is 20A RMS with 3.4 kW power. The THD of the injected grid current is 0.2%, which conforms to grid standards IEEE-519. The waveforms and measurements show that the proposed simplified PDPC is feasible and demonstrates good reference-tracking capabilities.

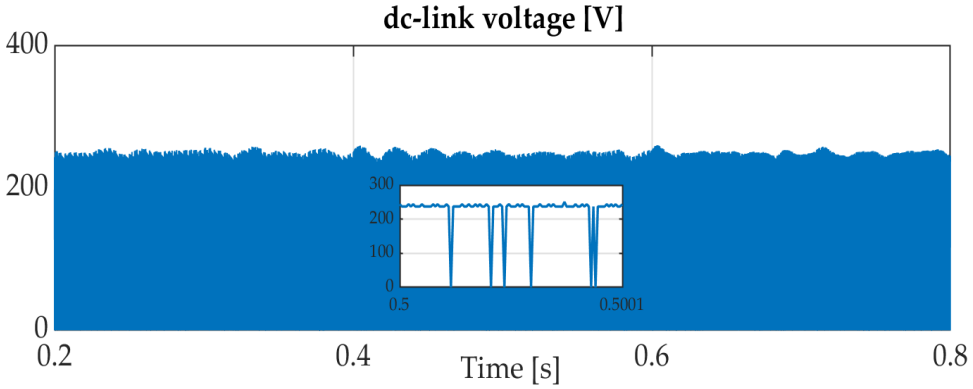


Figure 4.14: DC-link voltage.

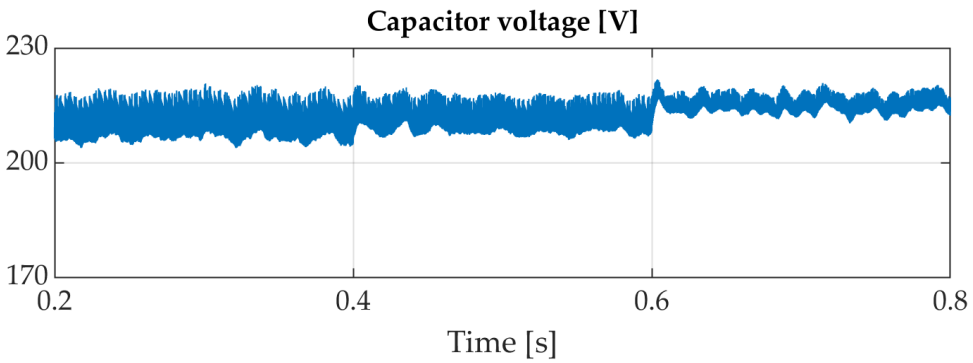


Figure 4.15: Capacitor C_1 voltage.

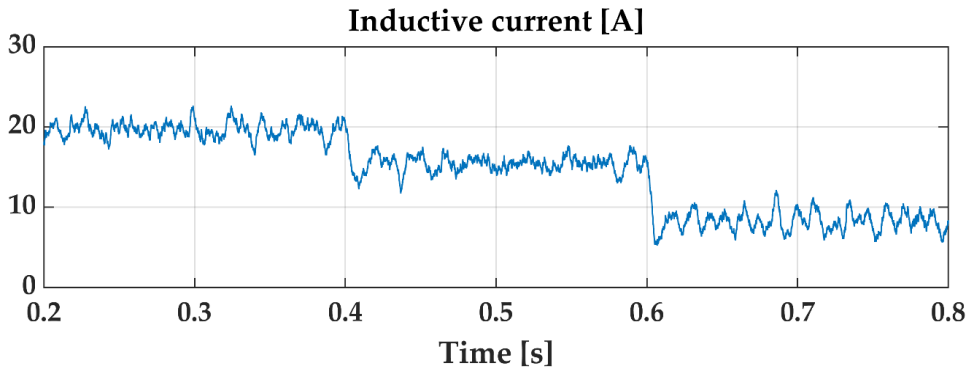


Figure 4.16: Inductor L_1 current.

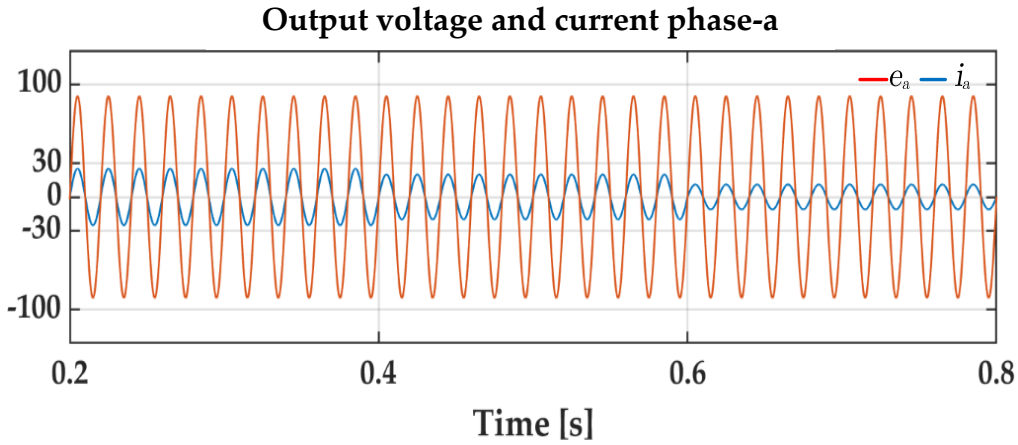


Figure 4.17: Output voltage and current in phase-*a*.

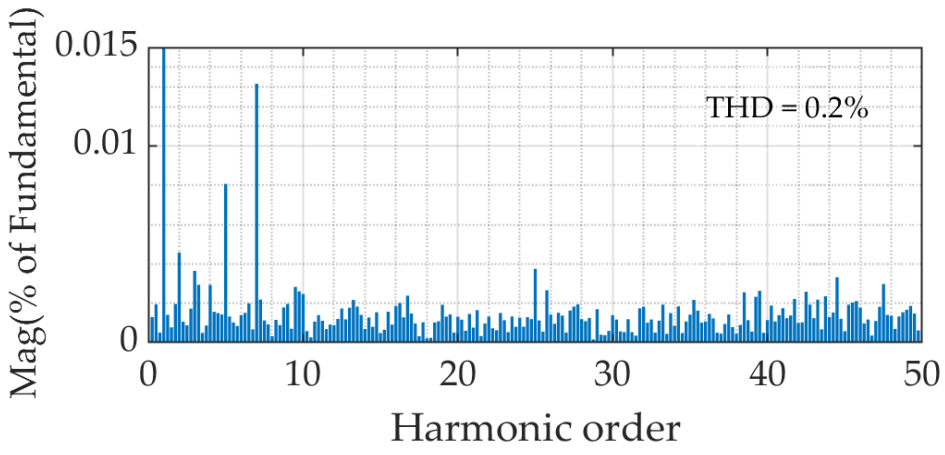


Figure 4.18: The *a*-phase current spectrum.

4.5 Comparative investigation

Table 4.4 presents a comparative investigation based on the complexity of the model, the output active power ripple, and the line current THD between the proposed simplified PDPC and recently published control schemes. The comparison is conducted on the same application, such as grid-connected mode. This comparison demonstrates that the proposed control methods efficiently enhance the line current quality with the Lower ripple in the injected active power.

Table 4.4. Comparison results between different control strategies.

Reference	Control Used		Modulation	Switching Frequency	Complexity	Power Ripple	THD %
	dc Side	ac Side					
[13]	Model Predictive Current Control With phase lock loop		No need	Variable Average of 22 kHz	High	Medium	3.20%
[14]	Model predictive control		No need	Variable Average of 9 kHz	High	Low	1.92%
[15]	Model predictive control		No need	Variable	High	Low	2.48%
[16]	Dead-beat control	Model Predictive Power Control	Optimal Sector Selection Method	Constant	Medium	Medium	2.27%
Proposed PDPC Method	PI controller	Model Predictive Power Control	Simplified space vector modulation	Constant 10 kHz	Low	Low	0.20%

4.5 HIL Validation Results

A hardware-in-the-loop (HIL) emulator was applied to evaluate and confirm our proposed control scheme for a three-phase grid-tied qZSI. The fundamental elements and signal channels of the HIL simulator for the proposed approach are shown in Figure 4.19.

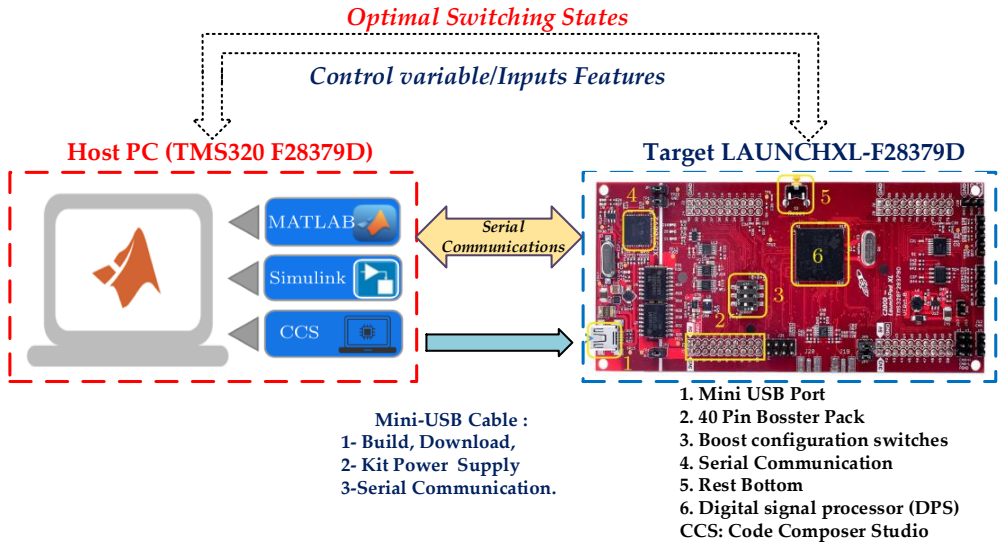


Figure 4.19: HIL simulator schematic for the proposed system.

In a usual HIL emulator, the three-phase grid-tied qZSI and its various PV irradiation are simulated and conducted on the personal computer (i.e., Host-PC) as a concept in MATLAB. However, the control strategies are carried out in an external target microcontroller kit (in our research, the C2000TM microcontroller-LaunchPadXL TMS320F28379D kit). The HIL emulator necessitates collaboration between the Host-PC and the target LAUNCHXL-F28379D, accomplished through a virtual serial COM port [25], [26]. In this case, the Host-PC sends measured signals (or input characteristics) such as V_{pv}, e_{abc}, and i_{abc} to the LAUNCHXL-F28379D kit. After receiving these signals from the target kit, the proposed control strategy designates the switching state for the next switching period. At last, the switching sequences are delivered to the Host-PC to control the qZSI switches and will be repeated at each sampling time T_s.

After configuring the devices and the Host-PC, as explained in [26], the HIL simulation is used to evaluate the effectiveness of the proposed control strategies in controlling the PV output voltage V_{pv}, the active output P, and reactive powers q. The system's operation under the dynamic response can be tested under different meteorological conditions. The studied conditions are 1000 W/m^2 and 800 W/m^2, respectively.

Figures 4.20- 21 show the active and reactive powers, and it can be seen that both injected powers track the reference under various solar irradiation.

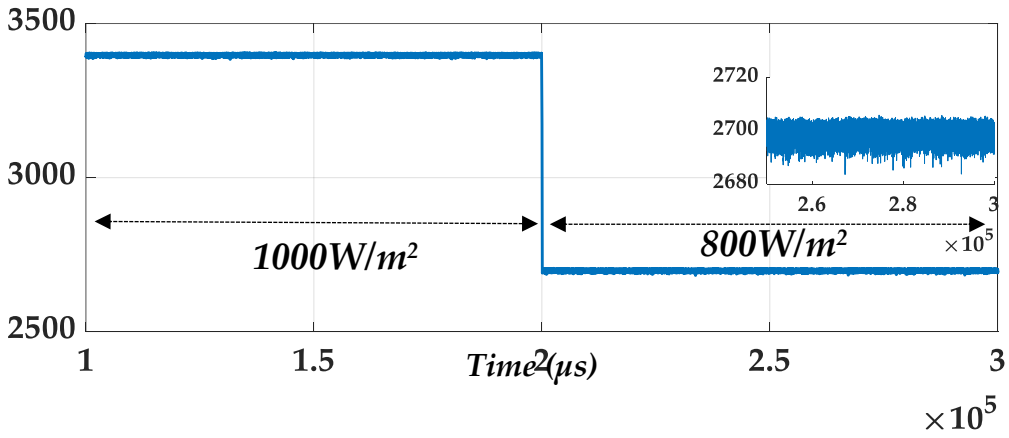


Figure 4.20 HIL validation: Output active power with a different level of irradiation

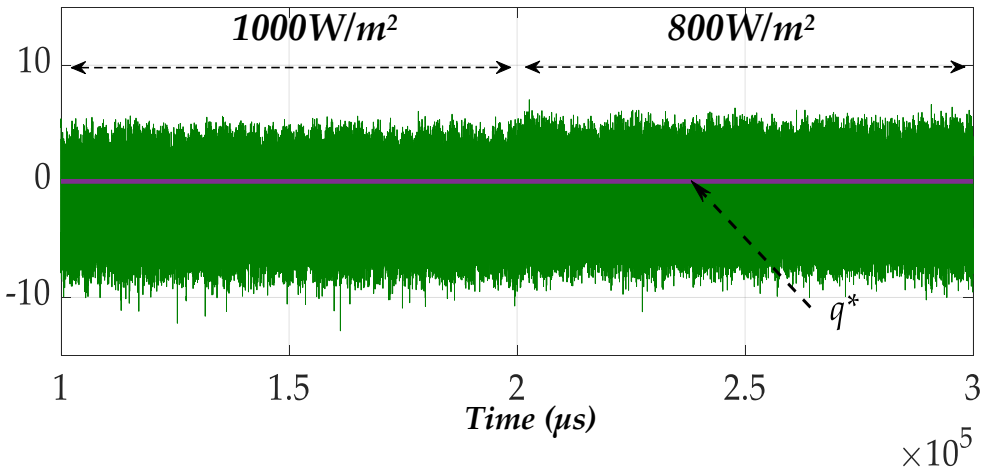


Figure 4.21 HIL validation**:** Reactive power under different levels of solar irradiation.

It is shown in Figure 4.22 that maintaining a dc-link peak voltage value through all the changing in the solar irradiation is due to adjusting the *ST* duty cycle.
In Figure 4.23, the output currents are almost sinusoidal and smoothly fluctuate. Moreover, it can quickly change during irradiation variations without producing overshoot or undershoot currents. Finally, the challenges among simulation and HIL findings are insignificant, demonstrating that the proposed simplified PDPC for grid-tied qZSI is successful in terms of implementations.

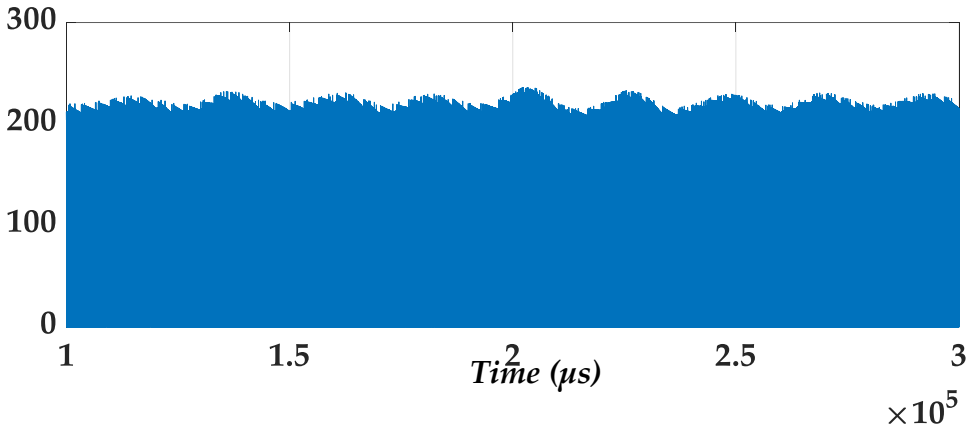


Figure 4.22: HIL validation: dc-link voltage.

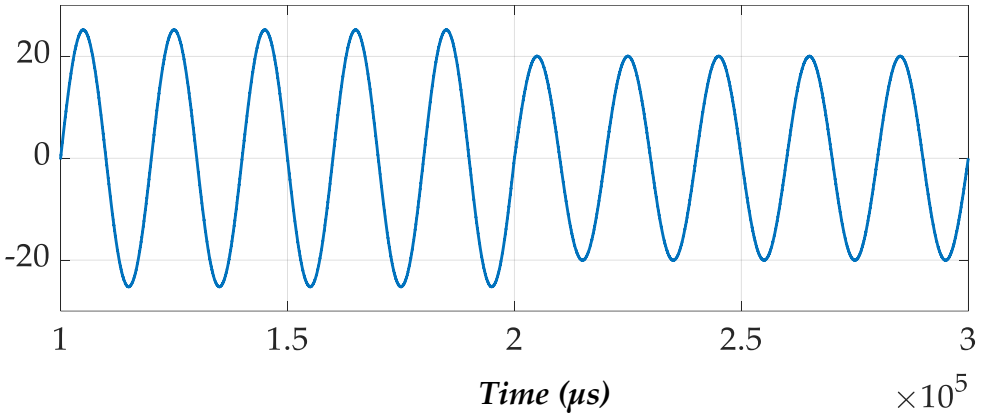


Figure 4.23: HIL validation: Output current in phase-*a*.

4.6. Summary

This chapter proposed a simplified PDPC with a fixed switching frequency for grid-tied qZSI. The suggested control strategy integrates the PDPC approach with the ZSVM block to function at fixed and low switching frequencies, improve system performance, and maintain the durability of its hardware devices. In addition, the simplified ZSVM is based only on the first sector calculation. It uses reference vector identification, *ON*-duration times calculation, and pluses generation with the *ST* state insertion. Consequently, it reduces the calculation time while increasing accuracy. The voltage reference vectors are also computed without the need for linear controllers. A PI controller adjusts the dc link voltage and the traditional P&O algorithm for generating V_{MPP} voltage reference. Finally, the simplified PDPC generates the voltage vector and switching pulses for the qZSI,

resulting in the smallest difference between predictive and reference values. The proposed simplified PDPC not only realizes the control of photovoltaic source voltage but also the optimal control of active and reactive powers on the ac side of the qZSI. The obtained results, and comparative evaluation, prove the effectiveness and feasibility of the proposed simplified PDPC in terms of reached grid *ac* voltage, active and reactive power regulation, and output current quality improvements. The HIL emulator was used to prove its feasibility on a DSP kit and illustrate its performance under varied irradiation levels.

4.7 Chapter references

[1] A. Chauhan and R. P. Saini, "A review on Integrated Renewable Energy System based power generation for stand-alone applications: Configurations, storage options, sizing methodologies and control," *Renew. Sustain. Energy Rev.*, vol. 38, pp. 99–120, 2014, doi: 10.1016/j.rser.2014.05.079.

[2] I. Grgić, M. Bašić, and D. Vukadinović, "Optimization of electricity production in a grid-tied solar power system with a three-phase quasi-Z-source inverter," *J. Clean. Prod.*, vol. 221, pp. 656–666, 2019, doi: 10.1016/j.jclepro.2019.02.245.

[3] W. Liang, Y. Liu, B. Ge, X. Li, F. J. T. E. Ferreira, and A. T. De Almeida, "Night operation, analysis, and control of single-phase quasi-Z-source photovoltaic power system," *IET Renew. Power Gener.*, vol. 13, no. 15, pp. 2817–2829, 2019, doi: 10.1049/iet-rpg.2018.6221.

[4] O. Ellabban, J. Van Mierlo, and P. Lataire, "Experimental study of the shoot-through boost control methods for the Z-source inverter," *EPE J.*, vol. 21, no. 2, pp. 18–29, 2011.

[5] M. Khatibi and S. Ahmed, "Z-source virtual synchronous generator: Operation and control," *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, pp. 97–104, 2021, doi: 10.1109/APEC42165.2021.9487373.

[6] S. Yan, Y. Yang, S. Y. Hui, and F. Blaabjerg, "A Review on Direct Power Control of Pulsewidth Modulation Converters," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 11984–12007, 2021, doi: 10.1109/TPEL.2021.3070548.

[7] Y. Gui, C. Kim, C. C. Chung, J. M. Guerrero, Y. Guan, and J. C. Vasquez, "Improved Direct Power Control for Grid-Connected Voltage Source Converters," *IEEE Trans. Ind. Electron.*, vol. 65, no. 10, pp. 8041–8051, 2018, doi: 10.1109/TIE.2018.2801835.

[8] S. Bayhan, H. Abu-Rub, and R. S. Balog, "Model predictive control of quasi-Z-source four-leg inverter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 7, pp. 4506–4516, 2016.

[9] M. A. Ismeil, A. Bakeer, and M. Orabi, "Implementation Quasi Z-Source Inverter for PV Applications Based on Finite Control Set-Model Predictive Control," *Int. J. Renew. Energy Res.*, vol. 9, no. 3, pp. 1462–1471, 2019.

[10] A. Bakeer, M. A. Ismeil, A. Kouzou, and M. Orabi, "Development of MPC algorithm for quasi Z-source inverter (qZSI)," in *2015 3rd International Conference on Control, Engineering & Information Technology (CEIT)*, IEEE, 2015, pp. 1–6.

[11] A. Bakeer and A. A. Ahmed, "Performance evaluation of PMSM based on model predictive control with field weakening operation and bidirectional quasi Z-source inverter," in *2017 Nineteenth International Middle East Power Systems Conference (MEPCON)*, IEEE, 2017, pp. 741–746.

[12] A. Bakeer, M. A. Ismeil, and M. Orabi, "Modified finite control set-model predictive controller (MFCS-MPC) for quasi z-source inverters based on a current observer," *J. Power Electron.*, vol. 17, no. 3, 2017, doi: 10.6113/JPE.2017.17.3.610.

[13] S. Jain, M. B. Shadmand, and R. S. Balog, "Decoupled active and reactive power predictive control

for PV applications using a grid-tied quasi-Z-Source inverter," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 6, no. 4, 2018, doi: 10.1109/JESTPE.2018.2823904.

[14] S. Sajadian, R. Ahmadi, and H. Zargarzadeh, "Extremum Seeking-Based Model Predictive MPPT for Grid-Tied Z-Source Inverter for Photovoltaic Systems," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 7, no. 1, pp. 216–227, 2019, doi: 10.1109/JESTPE.2018.2867585.

[15] S. Sajadian and R. Ahmadi, "Model predictive control of dual-mode operations Z-source inverter: Islanded and grid-connected," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 4488–4497, 2017.

[16] X. Duan, L. Kang, H. Zhou, and Q. Liu, "Multivector Model Predictive Power Control with Low Computational Burden for Grid-Tied Quasi-Z-Source Inverter Without Weighting Factors," *IEEE Trans. Power Electron.*, vol. 37, no. 10, pp. 11739–11748, 2022, doi: 10.1109/TPEL.2022.3174303.

[17] A. Bakeer, M. A. Ismeil, and M. Orabi, "A Powerful Finite Control Set-Model Predictive Control Algorithm for Quasi Z-Source Inverter," *IEEE Trans. Ind. Informatics*, vol. 12, no. 4, 2016, doi: 10.1109/TII.2016.2569527.

[18] A. Bakeer, G. Magdy, A. Chub, and D. Vinnikov, "Predictive control based on ranking multi-objective optimization approaches for a quasi-Z source inverter," *CSEE J. Power Energy Syst.*, vol. 7, no. 6, pp. 1152–1160, 2021, doi: 10.17775/CSEEJPES.2020.01310.

[19] M. Bouzidi, S. Barkat, A. Krama, and H. Abu-Rub, "Simplified predictive direct power control of three-phase three-level four-leg grid connected NPC converter," *IEEE Open J. Ind. Electron. Soc.*, vol. 3, pp. 448–459, 2022.

[20] A. Krama, L. Zellouma, B. Rabhi, S. S. Refaat, and M. Bouzidi, "Real-time implementation of high performance control scheme for grid-tied PV system for power quality enhancement based on MPPC-SVM optimized by PSO algorithm," *Energies*, vol. 11, no. 12, 2018, doi: 10.3390/en11123516.

[21] S. Ouchen, A. Betka, S. Abdeddaim, and A. Menadi, "Fuzzy-predictive direct power control implementation of a grid connected photovoltaic system, associated with an active power filter," *Energy Convers. Manag.*, vol. 122, no. August, pp. 515–525, 2016, doi: 10.1016/j.enconman.2016.06.018.

[22] W. Liu, Y. Yang, T. Kerekes, D. Vinnikov, and F. Blaabjerg, "Inductor Current Ripple Analysis and Reduction for Quasi-Z-Source Inverters With an Improved ZSVM6 Strategy," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 7693–7704, 2020.

[23] Y. Liu, B. Ge, H. Abu-Rub, and F. Z. Peng, "Overview of space vector modulations for three-phase Z-source/quasi-Z-source inverters," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 2098–2108, 2013.

[24] M. Bouzidi, S. Barkat, and A. Krama, "Simplified hybrid space vector modulation for multilevel diode clamped converter," *IET Power Electron.*, vol. 13, no. 17, pp. 3861–3870, 2020, doi: 10.1049/iet-pel.2020.0529.

[25] A. Bakeer, I. S. Mohamed, P. B. Malidarreh, I. Hattabi, and L. Liu, "An Artificial Neural Network-Based Model Predictive Control for Three-Phase Flying Capacitor Multilevel Inverter," *IEEE Access*, vol. 10, no. May, pp. 70305–70316, 2022, doi: 10.1109/ACCESS.2022.3187996.

[26] S. A. Zaid *et al.*, "From MPC-Based to End-to-End (E2E) Learning-Based Control Policy for Grid-Tied 3L-NPC Transformerless Inverter," *IEEE Access*, vol. 10, pp. 57309–57326, 2022, doi: 10.1109/ACCESS.2022.3173752.

Chapter 5

Conclusion and Future Outlook

5.1 Summary of contributions

This thesis has addressed the growing need for advanced control strategies in distributed generation systems, specifically focusing on the promising capabilities of ZSI/qZSIs as a type of impedance source inverter. The following chapters delve deeper into these contributions, providing detailed explanations, analyses, and simulation results to substantiate their effectiveness:

- **Chapter 2: Impedance Source Inverters: Exploring Topologies and Control Strategies** expands upon the comparative analysis from the introduction. It delves into the specific configurations of ZSI/qZSI with switched-inductors, analyzing their operating principles and performance characteristics. The chapter explores two modulation techniques (CZPWM, DZPWM) for three-phase ZSI/qZSIs, comparing their control complexity, efficiency, and suitability for different applications. Through detailed analyses and simulations, this chapter equips readers with the knowledge to select the most appropriate ISI configuration and control strategy for their specific needs.
- **Chapter 3: Optimized Modulation Scheme for Four-Leg quasi Z-Source Inverter** delves into the intricacies of the proposed 3DZSVM technique. It explains the three variations (3DZSVM2, 3DZSVM4, and 3DZSVM8) of the method and their specific advantages. The chapter provides a detailed breakdown of the benefits of the novel $\rho\sigma\tau$ coordinate system, explaining how it simplifies calculations and eliminates the need for trigonometric functions. It further explores the concept of single-sector operation and its contribution to optimizing pulse generation and time interval computations. This chapter will present extensive simulation results that validate the effectiveness of 3DZSVM for the 4L-qZSI compared to conventional methods, highlighting the improvements in steady-state performance and harmonic distortion reduction.
- **Chapter 4: Predictive Direct Power Control of qZSI for Grid-Tied PV Application** focuses on the practical implementation of the simplified PDPC strategy. It explains the underlying control principle and how the predictive

power model enables fixed switching frequency operation without a weighting factor. The chapter details the simplified space vector modulation technique used for selecting the optimal switching vectors and achieving superior power tracking and grid integration. This chapter will showcase simulation results that demonstrate the effectiveness of PDPC in a grid-tied PV system. The results will showcase the ability of PDPC to track maximum power from the PV source even with rapidly changing dynamics, while ensuring desired AC voltage output and precise control of active and reactive power with minimal power ripple.

The thesis investigates the potential of Impedance Source Inverters, particularly ZSI and qZSI configurations, for advanced control in distributed generation systems. It explores the operational principles and performance characteristics of these topologies, comparing modulation techniques like CZPWM and DZPWM. The thesis introduces a novel 3DZSVM technique for four-leg qZSI, leveraging the $\rho\sigma\tau$ coordinate system for simplified calculations and enhanced performance. It also focuses on the practical implementation of predictive direct Power control for qZSI in grid-tied PV systems, demonstrating its ability to track maximum power and ensure precise power control. By addressing the limitations of traditional inverters and offering innovative solutions, this research contributes to the advancement of efficient and reliable power systems.

5.2 Future Outlook

The research presented in this thesis opens exciting avenues for further exploration and development in the field of ZSI/qZSI control strategies for DG systems. Here are some potential areas for future research:

1. **Hardware Implementation and Experimental Validation**: While this dissertation extensively explored the proposed control strategies through simulations, the next crucial step is hardware implementation and experimental validation. This would involve building prototypes of the proposed ZSI/qZSI topologies and implementing the control algorithms on real-time digital signal processors (DSPs). Experimental results would provide valuable insights into the practical performance of the proposed methods, including factors like real-world hardware limitations and efficiency considerations.
2. **Advanced Control Techniques for Enhanced Performance**: This work focused on developing control strategies for specific objectives, such as maximizing power extraction and minimizing harmonic distortion. Future research could explore more advanced control techniques that incorporate additional functionalities. Potential areas of exploration include:

- ✓ Multi-objective Optimization: Develop control algorithms that simultaneously optimize multiple objectives, such as maximizing power output, minimizing THD, and improving system stability.
- ✓ Integration with Energy Storage Systems: Explore control strategies that seamlessly integrate ZSI/qZSI inverters with energy storage systems to enable features like peak shaving and power smoothing in DG systems.

3. **Grid Integration Challenges and Solutions**: As the penetration of DG systems increases, grid integration challenges become more prominent. Future research could investigate control strategies specifically designed to address these challenges, such as reactive power management and islanding detection.

By delving into these areas of future research, scientists and engineers can further refine and advance ZSI/qZSI technology, paving the way for its wider adoption in building robust and efficient Distributed Generation systems for a sustainable future.

Appendices

Appendix A

A.1 Parameters and specifications of 3L-qZSI

Circuit parametres	Value
qZSI network $C_{1,2}$, $L_{1,2}$	2,5 mF, 1mH
Filter inductance *Lf*, *rf*	3mH, 0.1 Ohm
Filter capacitor C_f	50 µF
inductive load *L*, *R*	12mH, 20 Ohm
Switching frequency f_S	10 KHz
Input DC voltage	160V~180V

A.2 Parameters and specifications of 4L-qZSI

Circuit parameters	Value
qZS network $C_{1,2}$, $L_{1,2}$	2,5 mF, 1mH
Internal resistance r_c, R_L	0.38 Ω, 0.1 Ω
Filter inductance L_f, r_f	3 mH, 0.1 Ω
Filter capacitor C_f	50 µF
Switching frequency f_s	10 kHz
Input dc voltage V_{in}	0 V13
Line frequency *f*	50 Hz

A.3 Photovoltaic module parameters.

Parameter	Value
Maximum power	150 W
Open circuit voltage	22.5 V
Short circuit current	8.75 A
The voltage at the MPP	18.25 V
Currently at the MPP	8.22 A
ΔV (P&O)	0.5 V
Sampling frequency (P&O)	100 Hz

A.4. System specifications 3L-qZSI system

Circuit Parameters	Value
qZS network $C_{1,2}$, $L_{1,2}$	1 mF, 4 mH
Internal resistance r_c, R_L	0.19 Ω, 0.1 Ω
Filter inductance L_f, R_f	mH, 0.1 Ω4
Switching frequency f_{Sw}	10 kHz
Sampling time T_s	10^{-6} s
Input PV voltage	180–185 V
Line frequency *f*	50 Hz
AC output voltage RMS	110 V

Appendix B

B. Power loss analysis using PLECS software

PLECS (Piecewise Linear Electrical Circuit Simulation), developed by Plexim, is a software tool specifically designed for simulating power electronics at the system level. However, it can be used for any electrical network analysis. Beyond electrical systems, PLECS offers the unique capability to model control systems and other physical domains, including thermal, magnetic, and mechanical aspects. Notably, PLECS includes a dedicated thermal modeling domain. This allows for accurate calculation of switching and conduction losses in electrical switches. The software utilizes multi-dimensional lookup tables based on manufacturer data or experimental measurements to achieve this precision. Thermal components reside in a separate section of the component library, while individual semiconductor components have built-in thermal descriptions accessible through a double-click.

To accurately represent real-world operation, the PLECS loss simulation model replicates the three-phase qZSI and four-leg qZSI configurations detailed in Figure C.1-2. This model enables the simulation of the auxiliary inverter system under realistic operating conditions and calculates the power losses within each switching device. The thermal models for the IGBTs and diodes used in the inverter are incorporated based on information obtained from their datasheets.

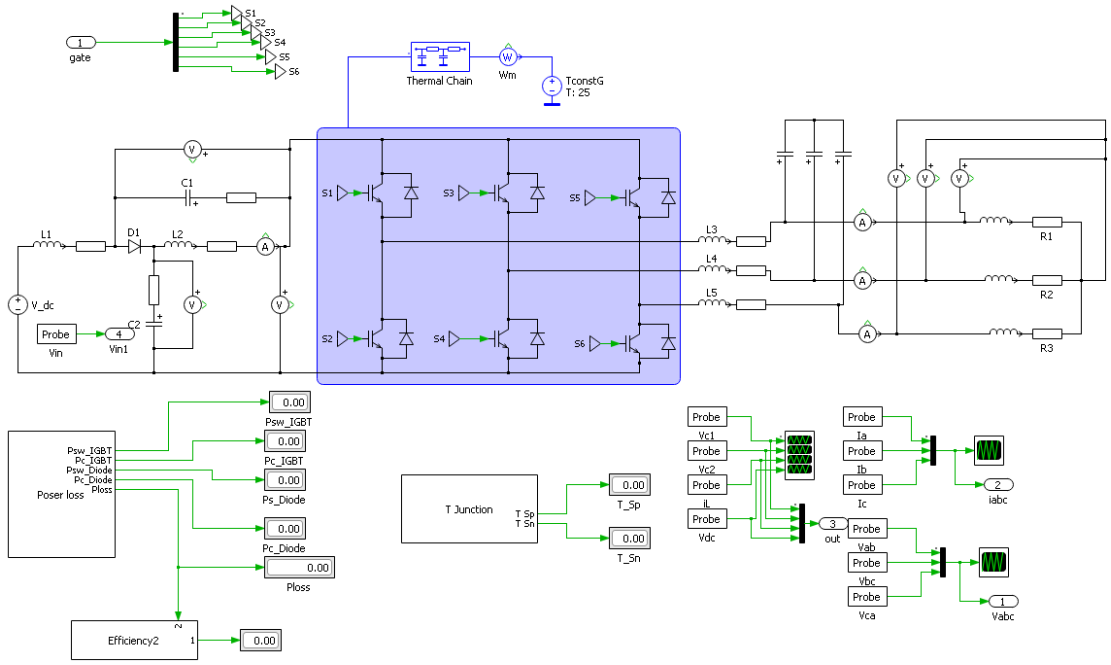


Figure (C.1): Simulation schematic of three-phase qZSI using PLECS.

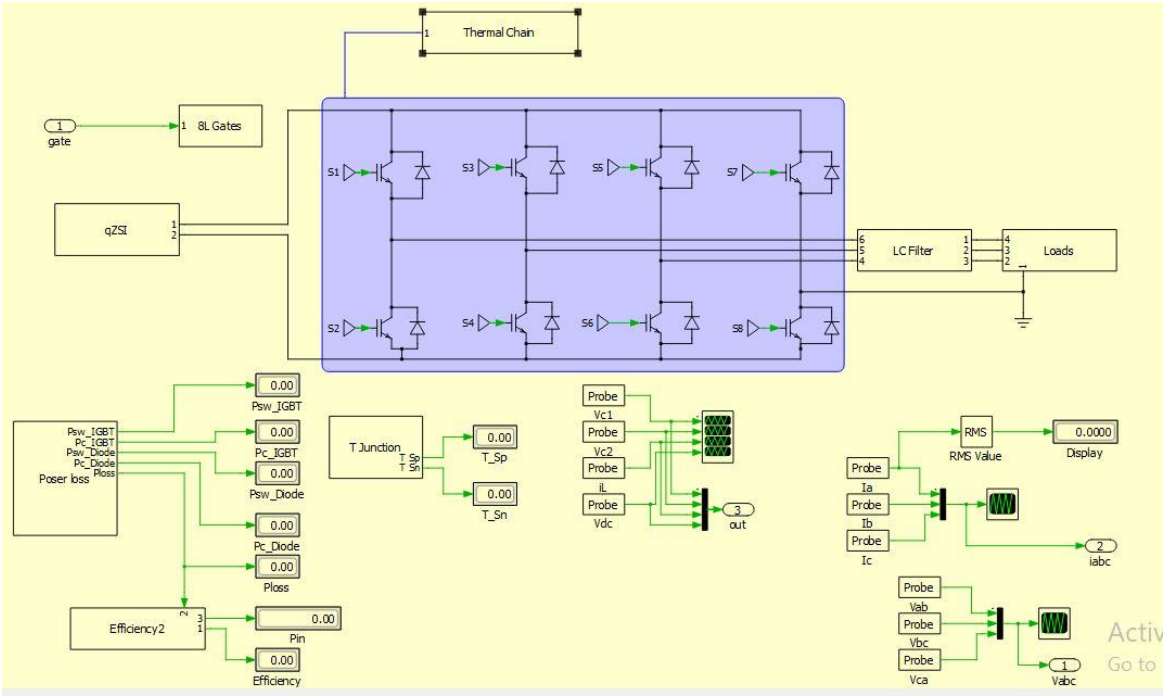


Figure (C.2): Simulation schematic of three-phase 4L-qZSI using PLECS.

The actual power losses experienced by the switching devices are directly linked to the circuit's operating conditions. PLECS calculates these losses by leveraging dedicated modules within its library, as illustrated in Figure (C.3). These modules can determine both the average conduction loss and the average switching loss for each device.

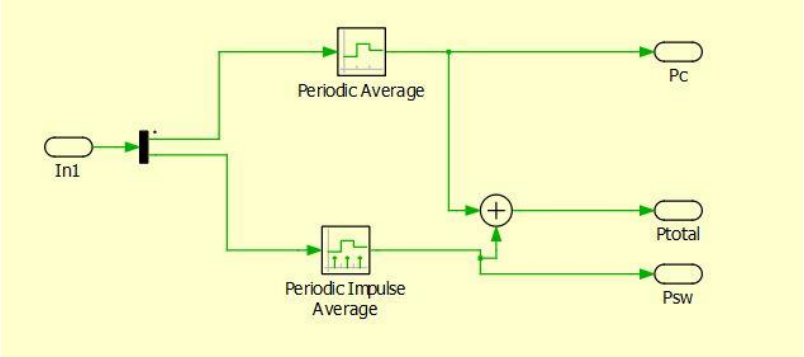


Figure (C.3): The power losses simulation model for each device IGBT and diode